

Table of Contents

18CSL37 : ANALOG AND DIGITAL ELECTRONICS LAB	2
A. LABORATORY INFORMATION	2
1. Lab Overview	2
2. Lab Content	2
3. Lab Material	3
4. Lab Prerequisites:	3
5. General Instructions	3
6. Lab Specific Instructions	4
B. OBE PARAMETERS	4
1. Lab / Course Outcomes	4
2. Lab Applications	5
3. Articulation Matrix	5
4. Mapping Justification	6
5. Curricular Gap and Content	6
6. Content Beyond Syllabus	6
C. COURSE ASSESSMENT	7
1. Course Coverage	7
2. Continuous Internal Assessment (CIA)	7
D. EXPERIMENTS	7
Experiment 01 :	7
Experiment 01 :	9
Experiment 02 :	.10
Experiment 02 :	.12
Experiment 03 :	.13
Experiment 04 :	.14

Note : Remove "Table of Content" before including in CP Book

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
AMGALORE T	Title:	Course Lab Manual	Page: 2 / 52

18CSL37 : ANALOG AND DIGITAL ELECTRONICS LAB

A. LABORATORY INFORMATION

1. Lab Overview

Degree:	BE	Program:	CS
Year / Semester :	2/3	Academic Year:	2018-19
Course Title:	Analog and Digital Electronics Lab	Course Code:	18CSL37
Credit / L-T-P:	2 / 1-0-2	SEE Duration:	180 Minutes
Total Contact Hours:	40 Hrs	SEE Marks:	60Marks
CIA Marks:	40	Assignment	1 / Module
Course Plan Author:	Prof. Geetha Megaraj/Rashmi K T	Sign	Dt :
Checked By:		Sign	Dt :



2. Lab Content

Unit	Title of the Experiments	Lab Hours	Concept	Blooms Level
1	a) Design and construct a Schmitt trigger using Op-Amp for given UTP and LTP values and demonstrate its working. b) Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working.	03	Analog Circuit Design	L4 Analyze
2	 a) Design and construct a rectangular waveform generator (Op-Amp relaxation oscillator) for given frequency and demonstrate its working. b) Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and demonstrate the change in frequency when all resistor values are doubled. 	03	Analog Circuit Design	L4 Analyze
3	Design and implement an Astable multivibrator circuit using 555 timer for a given frequency and duty cycle.	03	Analog Circuit Design	L4 Analyze
4	Design and implement Half adder, Full Adder, Half Subtractor, Full Subtractor using basic gates.	03	Combination al circuit design	L4 Analyze
5	 a) Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC. b) Design and develop the Verilog /VHDL code for an 8:1 multiplexer. Simulate and verify its working. 	03	Boolean expression realization	L4 Analyze
6	Design and implement code converter I)Binary to Gray (II) Gray to Binary Code using basic gates.	03	Code converters design	L4 Analyze
7	Design and verify the Truth Table of 3-bit Parity Generator and 4- bit Parity Checker using basic Logic Gates with an even parity bit.	03	Parity generator and Checker design	L4 Analyze
8	 a) Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table. b) Design and develop the Verilog / VHDL code for D Flip-Flop with positive edge triggering. Simulate and verify it's working. 	03	JK Master/ Slave flip flop realization	L3 Analyze
9	a) Design and implement a mod-n (n<8) synchronous up counter using J-K Flip- Flop ICs and demonstrate its working. b) Design and develop the Verilog / VHDL code for mod-8 up counter. Simulate and verify it's working.	03	counter design	L4 Analyze
10	Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate on 7-segment display (using IC- 7447).	03	counter design	L4 Analyze
11	Generate a Ramp output waveform using DAC0800 (Inputs are given to DAC through IC74393 dual 4-bit binary counter).	03	DAC realization	L4 Analyze

Logo	SK
	Doc C
SANGALORE *	Tit

SKIT	Teaching Process	Rev No.: 1.0
Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
Title:	Course Lab Manual	Page: 4 / 52

3. Lab Material

Unit	Details	Available
1	Text books	
		In Lib
2	Reference books	
		In dept
3	Others (Web, Video, Simulation, Notes etc.)	
		Not Available

4. Lab Prerequisites:

-	-	Base Course:		-	-
SNo	Course	Course Name	Topic / Description	Sem	Remarks
	Code				
1	15CSL37	Analog and Digital	Knowledge on basic gates.	2	
		Electronics Lab			
			Knowledge on Boolean expressions	2	

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

5. General Instructions

SNo	Instructions	Remarks
1	Observation book and Lab record are compulsory.	
2	Students should report to the concerned lab as per the time table.	
3	After completion of the program, certification of the concerned staff in-	
4	Student should bring a notebook of 100 pages and should enter the readings /observations into the notebook while performing the experiment.	
5	The record of observations along with the detailed experimental procedure of the experiment in the Immediate last session should be submitted and certified staff member in-charge.	
6	Should attempt all problems / assignments given in the list session wise.	
7	It is responsibility to create a separate directory to store all the programs, so that nobody else can read or copy.	
8	When the experiment is completed, should disconnect the setup made by them, and should return all the components/instruments taken for the purpose.	
9	Any damage of the equipment or burn-out components will be viewed seriously either by putting penalty or by dismissing the total group of students from the lab for the semester/year	
10	Completed lab assignments should be submitted in the form of a Lab Record in which you have to write the algorithm, program code along with comments and output for various inputs given	

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE *	Title:	Course Lab Manual	Page: 5 / 52

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Verify all the components and patch cords for their good working condition	
2	Make connections as shown in the circuit diagram	
3	Give supply to the trainer kit	
4	Provide input data to the circuit via switches and verify the truth table for	
	digital experiments	
5	Verify the output waveform on Cathode Ray Oscilloscope	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach.	Concept	Instr	Assessment	Blooms'
		Hours		Method	Method	Level
1	Design and analyze circuits schmitt trigger and rectangular waveform generator using operation amplifier IC and 555 IC	09	Analog Circuit Design	Instructi ons & Demons tration	Slip Test	L4
2	Design and analyze combinational circuits like adders, subtracters, parity generators and code converters using combination of gates	09	Combination al circuit design	Instructi ons & Demons tration	Slip Test	L4
3	Realize boolean expressions using multiplexer IC	03	Boolean expression realization	Instructi ons & Demons tration	Slip Test	L4
4	Realize JK master slave flip flop using nand gates	03	JK Master/ Slave flip flop realization	Instructi ons & Demons tration	Slip Test	L4
5	Design and analyze synchronous counter and asynchronous counters using combination of flip flops	03	Counter deign	Instructi ons & Demons tration	Slip Test CIA	L4
6	Generate ramp waveform by DAC using counter IC	03	DAC realization	Instructi ons & Demons tration	Slip Test CIA	L4
7	Understand simulation toolkit to design analog circuits	03	Analog Circuit simulation	Instructi ons & Demons tration	Slip Test CIA	L4
8	Understand simulation toolkit to design digital circuits	06	Digital Circuit simulation	Instructi ons & Demons tration	Assignment	L4
10						
11						
-	Total	42	-	-	-	-

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE T	Title:	Course Lab Manual	Page: 6 / 52

Copyright ©2017: cAAS. All rights reserved. Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

2. Lab Applications

SNo	Application Area	CO	Level
1	Waveform generators are used in signal generators	CO1	L4
2	Adders are used in Arithmetic logic unit	CO2	L4
3	Multiplexers are used in communication systems	CO3	L2
4	Flip flops are used in memory devices	CO4	L4
5	Counters are used in Digital clock	CO5	L4
6	Digital to analog converters are used in data transmission	CO6	L4
7	Simulation toolkits are used to design and test circuits	CO7,C	L3
		08	

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO1	PO2	PO3	PO	PO	PO	PO7	PO	PO	PO1	PO1	PO1	Level
					4	5	6		8	9	0	1	2	
CS501PC.1	Design and analyze circuits schmitt trigger and rectangular waveform generator using operation amplifier IC and 555 IC	2	2											L2
CS501PC.2	Design and analyze combinational circuits like adders, subtracters, parity generators and code converters using combination of gates	3	3											L2
CS501PC.3	Realize boolean expressions using multiplexer IC	2												L2
CS501PC.4	Realize JK master slave flip flop using nand gates	2	3											L3
CS501PC.5	2.5 Design and analyze synchronous counter and asynchronous counters using combination of flip flops													L2
CS501PC.6	Generate ramp waveform by DAC using counter IC		1											L2
CS501PC.7	Understand simulation toolkit to design analog circuits					2								L3
CS501PC.8	Understand simulation toolkit to design digital circuits					2								L2

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE *	Title:	Course Lab Manual	Page: 7 / 52

Copyright ©2017. cAAS. All rights reserved. Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Mapping		Mapping	Justification
Leve		Level	
СО	PO	-	-
CO1	PO1	2	Knowledge is required in construction of amplifiers and receivers
CO1	PO2	2	Analysis of amplifier and receiver circuits knowledge is required
CO2	PO1	3	Knowledge of adders and subtracters is required in design of ALU.
			Parity generators and code converters in communication systems
CO2	PO2	3	Adders and subtracters used to analyze ALU. Parity generators and code
			converters used to analyze communication systems
CO3	PO1	2	Knowledge is required in design of simplified circuits using multiplexer
CO4	PO1	2	Knowledge is required to build memory devices
CO4	PO2	3	To analyze memory devices flip flops are used
CO4	PO3	3	flip flops are used to design memory devices
CO5	PO1	3	Knowledge of counters helps the student to build timers and digital
			clocks
CO5	PO2	3	counters knowledge is required to analyze timers and digital clocks
CO5	PO3	2	counters are used to design timers and digital clocks
CO6	PO2	1	Knowledge is required to analyze working of communication systems
CO7	PO5	2	Use of simulation toolkit required to understand actual working of analog
			circuits
CO8	PO5	2	Use of simulation toolkit required to understand actual working of digital
			circuits

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Logo	
SANGALORE *	

SKIT	Teaching Process	Rev No.: 1.0
Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
Title:	Course Lab Manual	Page: 8 / 52

Copyright ©2017. cAAS. All rights reserved. Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teachi		No. of question in Exam						CO	Levels
		ng	CIA-1	CIA-2	CIA-3	Asg-1	Asg-2	Asg-3	SEE		
		Hours									
1	Schmitt Trigger	05	1	-	-	-	-	-	1	CO1	L4
2	Rectangular Waveform Generator	05	1	-	-	-	-	-	1	CO1	L4
3	Astable Multivibrator	03	1	-	-	-	-	-	1	CO1	L4
4	Full adder, Full Subtractor	03	-	1	-	-	-	-	1	CO2	L4
5	Multiplexer	05	-	1	-	-	-	-	1	CO3	L4
6	Binary to Gray	03	-	1	-	-	-	-	1	CO2	L4
7	Parity Generator and Checker	03	-	1	-	-	-	-	1	CO2	L4
8	JK Master slave Flip flop	05	-	-	1	-	-	-	1	CO4	L4
9	Synchronous Counter	05	-	-	1	-	-	-	1	CO5	L4
10	Asynchronous counter	03	-	-	1	-	-	-	1	CO5	L4
11	DAC0800	03	-	-	1	-	-	-	1	CO6	L4
-	Total	60	7	8	5	5	5	5	20	-	-

Note: Write CO based on the theory course.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	СО	Levels
CIA Exam – 1	25		
CIA Exam – 2			
CIA Exam – 3			
record	15		
Final CIA Marks	40	-	-

Logo	ſ
* QANGALORE *	

SKIT	Teaching Proces	S	Rev No.: 1.0
Doc Code:	SKIT.Ph5b1.F03		Date:07-08-2019
Title:	Course Lab Manual		Page: 9 / 52

-		
SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	05 Marks
2	Record Writing	10 Marks for each Expt
3	Internal Exam Assessment	25 Marks
4	Internal Assessment	40 Marks
5	SEE	60 Marks
-	Total	100 Marks



SKIT	Teaching Process	Rev No.: 1.0
oc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
Title:	Course Lab Manual	Page: 10 / 52

D. EXPERIMENTS Experiment 01 :

	TUTER	SKIT			Toochir	Procoss	
13			SKITI	Dhahi Eoo	reachin	ig i locess	Date:07-08-2010
	59	Title'		rigui.i Ug salah Mar			Date:07-00-2019
Conud	GALORE		Cours		iuut		1 aye. 11 / 52
-	Expe	riment No.:	1a	Marks		Date Planned	Date Conducted
1	Title		Schm	nitt Trigger			
2	Course	Outcomes	Desig gene	yn and ar rator using	nalyze circu operation ar	its schmitt nplifier IC an	trigger and rectangular waveform d 555 IC
3	Aim		Desig and L	gn and imp _TP values.	lement the S	Schmitt Trigg	er using µA741 Op-Amp or given UTP
4	Materia Equipm	l / Ient Required	Opan Signa	np,Resistor al generato	rs,DC regulat r,CRO,Conne	ed power su ecting wires,0	pply,Dual power DC power supply CRO probes,Bread Board
5	Theory, Principl	Formula e, Concept	DESIC From point UTP= VCC LTP = Henc the fc UTP -	GN theory of $\frac{R1Vref}{R1+R2}$ $= \frac{R1Vref}{R1+R2}$ the given the bollowing defined the LTP = $\frac{2R}{R}$ $= LTP = \frac{2R}{R}$	Schmitt trig $\frac{F}{r} + \frac{R2V s at}{r1+r2}$ $\frac{F}{r} - \frac{R2V s a}{r1+r2}$ $e LTP & UTF$ $e LTP & UTF$ $\frac{1Vr ef}{1+R2}$ $\frac{2R1V s at}{R1+R2}$	ger circuit u - Vsat is pos <u>t</u> (1) (2)	sing op-amp, we have the triggering itive saturation of the opamp =90% of nd the values R1,R2 and Vref values,
			Let V R2= 1 (UTP From Vref=	'sat = 10V, l o KΩ R1=9 + LTP) + equation (((UTP+)	JTP = 4V & L go KΩ 1) we have LTP)(R1+2 2 R1	TP = 2V, then <u>R2))</u> =3.33 V	equation (2) yields R1=9R2
6	Proced Activity Pseudc	ure, Program , Algorithm Code1	1)Cor 2)Set 3)Set 4)App signa 5)obs 6)Usi	nect the c +Vcc and - Vref as pe oly Vin a s I generato serve the Ir ng XY moc	ircuit as show Vcc to +12V r the design. inusoidal sig r. iput and outp le observe th	vn the diagra and -12V res Jnal of frequ put waveforn he hysteresis	im. pectively ency around 500Hz 10Vpp from the ns on the CRO curve.
7	Block, Diagrar Equatic Graph	Circuit, Model n, Reactior n, Expectec		$V_{\rm in}$	$ \begin{array}{c} 2 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1$		

Logo		SKIT	Teaching Process	Rev No.: 1.0
		Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
ES T OAL		Title:	Course Lab Manual	Page: 12 / 52
Copyrie	ght ©2017. cA	AS. All rights reserved.		
8	Observa	ation Table,		
	Look-u	p Table		
	Output			
9	Sample	Calculations		
	0	0.1.1.1.		
10	Grapns,	Outputs	(A) Schmitt Trigger (active)	n ha nak
			HELDS 100 - WIGHT +Viet +Viet	
			20 22 LTP	4V
			-10V os 10ms 20ms 30ms 40ms	
			- V(0100T) Time	
			Designed value of UTP = 4V	
			Designed value of LTP = 2V	
			Designed value of Hysteresis = 2 V (UTP – LTP)	
	D 11	0 A L .		
11	Results	& Analysis		
12	Applica	tion Arooc	Wayoform gonorators are used in signal gonorators	
12	Pomarl		waveronni generators are used in signat generators	
13		Cianatura		
14		Signature		
11 12 13 14	Results Applica Remark Faculty with Da	& Analysis tion Areas s Signature te	Waveform generators are used in signal generators	

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE *	Title:	Course Lab Manual	Page: 13 / 52

Experiment 01:

SP.MP	000	SKIT	Teaching Process			Rev No.: 1.0	
		Doc Code:	SKIT.Ph5b1.F03	¥			Date:07-08-2019
Es C		Title:	Course Lab Mar	nual			Page: 14 / 52
Copyri	CALORE	AS All rights reserved					
_	Expe	riment No.:	1b Marks		Date	D	ate
	Слре				Planned	Conc	lucted
1	Titlo		Schmitt Triagor		rannea	COIR	
2	Courco	Outcomos	Decign and imr	alomont a Sok	mitt triago	rucing On Amn	using a simulation
2	Course	Outcomes	Design and imp		inniti trigger	r using op-Amp	using a simulation
) Sels	monstrata i	ta warkina	
	A :					LS WURKING.	
3	Aim		Design and imp	olement a Scr	imitt triggei	r using Op-Amp	using a simulation
) Sels	un a la atrata la	to weatling	
	N 4 - 1 1 -		OF UTP and LTP	values and de	emonstrate	ls working.	
4	Materia	l /	1. uA 741				
	Equipm	ient Required	2. resistors 10k, 9	90k			
		3. vdc 3.3 , 10					
			4. voltages				
			5 ground of sol	urce			
			6. designing sof	tware			
5	Theory,	Formula	DESIGN				
	Principl	e, Concept	From theory of	Schmitt trigge	er circuit us	ing op-amp, we	have the triggering
			points,				
			R1Vref	$\frac{R2Vsat}{1}$	Veat is nosi	tive saturation of	the onemn -00% of
			R1+R2	r1+r2	v sat 13 posi		
			VCC				
			R1Vret	R2Vsat			
			$LTP = \frac{D1}{D1}$	$-\frac{112}{n11n2}$			
			KI+KZ	11+12			
			Honco aivon th		values to fir	d the values D1	Da and Vrof values
			the following design is used				
			une ioliowing de	1 V			
			$UTP + ITP = \frac{2R}{2R}$	<u>1vref</u>	(1)		
			R	1 + <i>R</i> 2	(=)		
				2R1Vsat	(-)		
			OIP - LIP = -	R1+R2	(2)		
			l et Vsat = 10V l		P = 2V then e	equation (2) vields	s R1=0R2
			R2= 10 KO R1=0			equation (2) yield	STAT SILE
				90102			
			From equation (1) we have			
)))		
			Vref=		2)) =3.33 V		
				2 <i>R</i> 1			
6	Proced	ure, Program	1. design the cir	cuit as shown	the diagram	٦.	
	Activity	, Algorithm	2. Set vdc value	s and resistor v	values		
	Pseudo	Code1	3. connect 0 sou	arce ground co	onnection		
			4. place the wire	es and design a	as per giver	n in circuits	
			5. set Run to tim	e: 40msec	-		
			6. set step size:).1msec			
			7 run the proje	ct design to ge	et the expec	ted waveform.	

35 101	ogo	SKIT	Teaching Process	Rev No.: 1.0
		Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
5 × 84	2 ALORE	Title:	Course Lab Manual	Page: 15 / 52
Copyri	ght ©2017. cA	AS. All rights reserved	· · · · · · · · · · · · · · · · · · ·	
7	Block, (Circuit, Mode	R2 R1 90k	
	Equation	i, Reaction n Expected	F 105-	
	Graph	I, Expected		
			2 - 5 OS11	
			VOFF = 0V VAMPL = 10V	
			FREQ = 50Hz V4 V2 10Vdc	
		···	=0	
8	Observa	ition Table	,	
	Output		•	
9	Sample	Calculations		
10	Crapha	Outouto		
10	Graphs,	Outputs		
			Us 10µs 20µs 30µs 40µs 50µs Time	
			Designed value of UTP = 4V	
			Designed value of Hysteresis = 2 V (UTP – I TP)	
11	Results	& Analysis		
12	Applicat	ion Areas	Waveform generators are used in signal generators	
13	Remark	S Classic		
14	Faculty	Signature		
	with Dat	e		

Logo	SKIT	Teaching Process	Rev No.: 1.0				
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019				
SA ANGALORE T	Title:	Course Lab Manual	Page: 16 / 52				
Copyright ©2017. cAAS. All rights reserved.							

Experiment 02 :

Logo	SKIT	Teaching Process	Rev No.: 1.0					
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019					
ST CANGALORE *	Title:	Course Lab Manual	Page: 17 / 52					
Copyright ©2017. cAAS. All rights reserved.								

* SANGALORE *	l itle:	C

-	Experiment No.:	2	Marks		Date		Date	
1	Titlo	Doot		form conorat	Planned	rolovation		
2	Course Outcomes	Desic	in and analyz	ze circuits Sch	nmitt triager	and rectanc	ular wavefor	m generator
-		using	operation a	mplifier IC and	d 555 IC	anarootang		in generator
3	Aim	To c	lesign and	implement t	he rectang	ular wavefo	orm generato	or (Op-Amp
		relaxa	ation oscillat	or) for given f	requency			<u> </u>
4	Material / Equipment Required	Opan wires	wires,CRO probes,Bread Board					
5	Theory, Formula, Principle, Concept	The p	The period of the output rectangular wave is given as T2 RC ln $\frac{1+B}{1-B}$ (1)					
		Whei	Where, $B = \frac{R1}{R1+R2}$ is the feedback fraction					
		lf R 1 Anotł	= R 2 , then fr ner example,	rom equation if R 2 =1.16 R	(1) we have 1 , then T = 2	T = 2RC ln(3) RC	-(2)	-3 =
		Exarr Use F	ple: Design f R 2 =1.16 R 1, f	for a frequence for equation (2	cy of 1kHz (in 2) to be appl	nplies T= 1 ied.	./f = 1/10 = 10	0 = 1ms
		Let k figure Choo	2 1 = 10K(2, tr 2) 50 povt 2 val	1en R 2 = 11.6	kΩ (use 20k	Ω potention	from oquation	wn in circuit
		CHOO	se hext a val		10	e value of R	nomequatio	11 (∠).
		Let C	=0.1µF (i.e., 10) -7), then R=	$T/2C = \frac{1}{2*1}$	<u>0</u> =5KΩ		
		The voltage across the capacitor has a peak voltage of $\frac{R1}{R1+R2}$ Vsat						
6	Procedure, Program Activity	1. Cor 2 Set	nect the circ +Vcc and -V	cuit as shown /cc to +12\/ an	the diagram). Actively		
	Algorithm, Pseudo	3. obs	serve the out	put waveforr	ns on the CR	0		
	Code	4. No	te down the	Period T on	the time sc	ale on the C	CRO and hen	ce compute
-	Plack Circuit	the F	requency.					
/	Model Diagram,							
	Reaction Equation,		¥ 0.1 μ ²	$+V_{cc}$ +15V V _c				
	Expected Graph		$R_1 \qquad V_1$					
		$10 \text{ K}\Omega \qquad 5 -15V \qquad \qquad$						
			₹	11.6 KΩ (20-K Pot)				
8	Observation Table							
	Look-up Table,							
	Output							
9	Sample							
	Calculations							

300	ogo	SKIT	Teaching Process	Rev No.: 1.0
		Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
ST BAN	CALORE +	Title:	Course Lab Manual	Page: 18 / 52
Copyrig	ght ©2017. cA	AS. All rights reserve	ed.	
10	Graphs,	Outputs	v_{cont}	
11	Results	& Analysis		
12	Applicat	tion Areas		
			Waveform generators are used in signal generators	
13	Remark	S		
14	Faculty with Dat	Signature te		

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE *	Title:	Course Lab Manual	Page: 19 / 52

Experiment 02 :

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SA PANGALORE + C	Title:	Course Lab Manual	Page: 20 / 52
Copyright ©2017, cA	AS. All rights reserved		

-	Experiment No.:	2b	Marks		Date		Date	
1	Titla	Recta	angular wave	form genera	tor (On-Amn	relayation c	scillator)	
2	Course Outcomes	Desic	angular wave	ement a rect	angular way	eform gene	rator (Op-Am	n relaxation
		oscill	ator) using a		angular wav	eronn gene		pretaxation
		simul	lation packad	ge and demo	onstrate the o	hange in fre	equency where	n all resistor
		value	s are double	d.		9	()	
3	Aim	То с	lesign and	implement	the rectang	ular wavefo	orm generato	or (Op-Amp
		relax	ation oscillat	or) for given	frequency			
4	Material /	1. uA	741					
	Equipment	2. res	istors 10k, 10	k				
	Requirea	3. va	5 3.3 , 10 tagas					
		4. VOI 5. arc	und '0' sourc	`e				
		6. Ca	pacitor 0.1					
		6. de:	signing softw	vare				
5	Theory, Formula, Principle, Concept	The p	period of the	output recta	ngular wave	is given as T	$2 RC ln \frac{1+l}{1-l}$	<u>B</u> (1)
		Whei	re, B= $\frac{R1}{R1+R}$	$\frac{1}{2}$ is the fee	dback fractic	n		
		lf R 1 Anotl	= R 2 , then fi her example,	om equatior if R 2 =1.16 R	1 (1) we have 1 , then T = 2	T = 2RC ln(3) RC	-(2)	2
		Example: Design for a frequency of 1kHz (implies $T = 1/f = 1/10^3 = 10^3 = 1$ ms Use R 2 = 116 R 1 for equation (2) to be applied						
		Let F	$R = 10k\Omega$, th	ien R 2 = 11.0	$\delta k\Omega$ (use 20k	Ω potentior	neter as show	wn in circuit
		Choo	se next a val	ue of C and I	hen calculat	e value of R	from equation	n (2).
					т (ас 10			
		Let C	,=0.1µF (I.e., 10) - /), then R=	= 1/2C = <u>2*1</u>	$0^{=5K\Omega}$		
		The \	oltage acros	s the capaci	tor has a pea	k voltage of		
		R	1 Vcat					
		$\overline{R1+R2}^{Vsat}$						
6	Procedure,	1. Cor	nnect the circ	cuit as showr	n the diagram	٦.		
	Program, Activity,	2. Set	+Vcc and -V	cc to +12V ar	nd -12V respe	ectively		
	Algorithm, Pseudo	3. ODS	serve the out	put wavefor	ms on the CF	(U alo on tho (DO and hone	co computo
	Code	the F	requency.	Fellou I OI				ce compute
7	Block, Circuit,		R3	R1 10k				
	Model Diagram,			V1 10Va	Ic			
	Reaction Equation,				1.0			
	Expected Graph		3	+ 052				
				J> OS1	`			
			=0		1.0	4		
				rk2 1k				
8	Upservation Table,							
	Output Table,							
a	Sample							
	Calculations							

STATE OF	OGO	SKIT	Teaching Process	Rev No.: 1.0
		Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
to t BA	CALORE +	Title:	Course Lab Manual	Page: 21 / 52
Copyri	ght ©2017. c/	AS. All rights reserve	ed.	
10	Graphs	Outputs	(A) Relaxation Oscillator (active) ov -100 0 0 0 (Uli-) 100 0 0 0 (Uli-) 100 0 0 0 0 (Uli-) 100 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	
11	Results	& Analysis		
12	Applica	tion Areas		
			Waveform generators are used in signal generators	
13	Remark	(S		
14	Faculty with Da	Signature te		

Logo	SKIT	Teaching Process	Rev No.: 1.0		
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019		
SA ANGALORE T	Title:	Course Lab Manual	Page: 22 / 52		
Copyright ©2017. cAAS. All rights reserved.					

Experiment 03:

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SA ANGALORE T	Title:	Course Lab Manual	Page: 23 / 52

SANGALORE	THUS.	00
Copyright ©2017. c/	AAS. All rights reserved.	

-	Experiment No.:	1	Marks		Date		Date	
1	Title		imer		Planned		conducted	
2	Course Outcomes	Desig	gn and analyz	ze circuits sc	hmitt trigger	and rectang	ular wavefor	m generator
3	Aim	To c relax	lesign and ation oscillate	implement or) for given t	the rectang frequency	ular wavefo	orm generat	or (Op-Amp
4	Material / Equipment Required	Time CRO,	r IC 555,Resis Connecting \	stors,Capacit wires,CRO pr	or,DC regula obes, Bread	ited power s Board	upply,Signal	generator &
5	Theory, Formula, Principle, Concept	DESI Giver The t When From t H = t L = (T = t I Duty Let C R B = The \ capa Note 100% Exam choo	GN infrequency (ime period T re t H is the ti the theory c 0.693 R B C - 0.693 (R A + R H + t L = 0.693 cycle = t H / 5.8KΩ (from /cc determin citor voltage : The duty c . If R A is muc aple 2: freque se R A = 6.8kt	f) = 1KHz and =1/f = 1ms = ime the outp of Astable mu (1) R B)C(2 3 (R A +2 R B) T = 0.6. Hence ubstituting in equation 1) a les the upper waveform) a ycle determ ch smaller the ency = 1kHz Ω and R B = 3	duty cycle = t H + t L ut is high and iltivibrator us) C ce t H = 0.6T the above e and R A = 2.9k r and lower the s UT = CC ~ I ined by R A an R B , the c and duty cy 3.3kΩ.	60% (=0.6) d t L is the tir sing 555 Time = 0.6ms and quations, (Ω (from equ hreshold vol LT = CC . & R B can duty cycle ap (cle =75%, R	ne the outpu er, we have t L = T – t H = ation 2 & R B tages (observ vary only be pproaches 50 A = 7.2kΩ &	t is low. 0.4ms. values). ved from the etween 50 & %. R B =3.6kΩ,
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Cor 2. Set 3. ob: 4. No comp	nnect the circ +Vcc to +5V serve the out te down the pute the perio	cuit as showr put wavefor Period Ton a od T and Free	n the diagram ms on the CF and Toff on t quency f.	n. RO he time scal	e on the CR() and hence
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	5.00		Aty Cycle. 8 V _{cc} Re V _{cc} Re 0 0 0 0 0 0 0 0 0 0 0 0 0	4 +V _{CC} 3 5 5 3 0 0 0 0 0 0 0 0 0 0 0 0 0			
8	Observation Table, Look-up Table, Output							
9	Sample							
10	Graphs, Outputs		CAP# WAV	ACITOR E FORM	v			
CS					·LT		٨	ad Datab
rep	bared by			O/P	t _L		Approv	vea. Patch
				<u> </u>				

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE *	Title:	Course Lab Manual	Page: 24 / 52
Copyright ©2017.	cAAS. All rights reserved	1.	

opyri	ght ©2017. cAAS. All rights reserve	ed.
11	Results & Analysis	
12	Application Areas	Waveform generators are used in signal generators
13	Remarks	
14	Faculty Signature with Date	

Logo	SKIT	Teaching Process	Rev No.: 1.0		
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019		
SA ANGALORE T	Title:	Course Lab Manual	Page: 25 / 52		
Copyright ©2017. cAAS. All rights reserved.					

Experiment 04 :



Logo	SKIT	Teaching Process	Rev No.: 1.0			
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019			
SA RANGALORE +	Title:	Course Lab Manual	Page: 27 / 52			
Convright ©2017 CAAS All rights reserved						

Copyri	ght ©2017. cAAS. All rights reserv	ed.
Copyri	gnt ©2017. CAAS. All rights reserv	ed.
9	Sample	
	Calculations	
10	Graphs, Outputs	Respective Truth tables are verified
11	Results & Analysis	
12	Application Areas	Adders and subtracters are used in arithmetic logic unit
13	Remarks	
14	Faculty Signature	
	With Date	

Logo	SKIT	Teaching Process	Rev No.: 1.0		
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019		
SA ANGALORE T	Title:	Course Lab Manual	Page: 28 / 52		
Copyright ©2017. cAAS. All rights reserved.					

SKIT Teaching Process Rev No.				Rev No.: 1.0				
		Doc Code:	SKI	SKIT.Ph5b1.F03 Date:07-08				
S* BAN	Title:		Cοι	ırse Lab Mar	Page: 29 / 52			
Copyrig	ght ©2017. cA	AS. All rights reserv	ed.			.		•
-	Exper	iment No.:	5a	Marks		Date	Da	ate
1	Title		Multir	lexer		Flaimed	Conc	
2	Course	Outcomes	Desig	n and ana	lyze combin	ational circu	its like adders,	subtracters, parity
			genei	rators and co	de converte	rs using com	bination of gates	
3	Aim		Given	a 4-variable	e logic expre	ssion, simplif	y it using Entered	d Variable Map and
		1 /	realiz	e the simplif	ied logic exp	ression using	8:1 multiplexer IC	
4	Materia	l /	1 IC 7	4LS151 ch.chords				
	Reauire	ed	2. Fat 3.Pox	/er chords				
			4.Trai	ner Kit				
5	Theory,	Formula,						
	Principl	e, Concept						
6	Proced	ure, A ativity	1.Ver	ify all co	mponents	and patch	chords whet	her they are in
	Algorith	n, Activity, m Pseudo	good	1 condition	n or not.			
	Code		2. Mal	<pre><e <="" connection="" pre=""></e></pre>	ons as shown	in the circuit	diagram.	
			3. GIV 4. Pro	yide input d	ne trainer kil.	Luit via switch		
			5. Ver	ify truth tabl	e sequence a	and observe of	output	
7	Block,	Circuit,	-	_,	•		·	
	Model	Diagram,				4 00 7415	51	
	Reactio	n Equation, ad Graph				3 D1	Y 5	-Output
	Expecte	eu Graph				2 D2 V		vcc
					L	15 D3	GND 8	
				HI		14 D5	G 7	
						13 D6		0
					τ	12 D7 С В	A	
						11 10	9	
						0 2		
		-+: T-l-L-						
8	Upserva Look-ui	alion Table, n Table		Decim A	B C D f	MEV map	7	
	Output			al		entry		
				0 0	0 0 0 0	$0 \Box D0$		
				1 0 2 0	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	1 □D1	-	
				$\frac{2}{3}$ 0	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\Gamma \Box D\Gamma$		
				4 0	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	1 □D2	-	
				5 0	1 0 1 1			
				6 0	1 1 0 0	$0 \square D3$		
				7 0	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		-	
				$\frac{0}{9}$ 1	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\Lambda \sqcup D4$		
				10 1	0 1 0 X	X □D5	-	
				11 1	0 1 1 X			
				12 1	1 0 0 0	$D \square D6$		
				13 1 14 1	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		-	
				15 1	$1 1 0 0 \\ 1 1 1 1 1$			
9	Sample							
	Calcula	tions	Der		toble ·	wife a d		
10	Graphs,	Outputs	Respe	ective I ruth	tables are ve	rifiea		

	ÖĞO	SKIT	Teaching Process	Rev No.: 1.0	
		Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019	
	S × BANG	GALORE	Title:	Course Lab Manual	Page: 30 / 52
С	Copyrig	ht ©2017. cÅ	AS. All rights reserve	d.	·

11	Results & Analysis	
12	Application Areas	Adders and subtracters are used in arithmetic logic unit
		3
13	Remarks	
14	Faculty Signature	
	with Date	



SKIT	Teaching Process	Rev No.: 1.0
Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
Title:	Course Lab Manual	Page: 31 / 52

-	Experiment No.:	5b	Marks		Date Planned		Date Conducted	
1	Title	Multip	fultiplexer					
2	Course Outcomes	Desigı verify	esign and develop the Verilog /VHDL code for an 8:1 multiplexer. Simulate and erify its working					
3	Aim	Verilo	g /VHDL co	de for an 8:1 i	multiplexer			
4	Material / Equipment Required	1.	1. Designing tool software					
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. 2. 3. 4. 5. 6.	Create a n Create a n Create a n Enter the u Create a n Type the c	ew project ew workshee ew blank pag user name an ew VHDL sou code as given	et ge d input outpu urce	ıt variable d	etails	
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output							
9	Sample Calculations							
10	Graphs, Outputs	Respe	ective Truth t	ables are ver	ified			
11	Results & Analysis							
12	Application Areas	Adder	s and subtra	acters are use	ed in arithmeti	ic logic unit		
13	Remarks							
14	Faculty Signature with Date							

Logo	SKIT	Teaching Process	Rev No.: 1.0		
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019		
SA CANGALORE +	Title:	Course Lab Manual	Page: 32 / 52		
Copyright ©2017. cAAS. All rights reserved.					

W	OCO	SKIT			Teach	ing Process	5		Rev N	0.:10	
		Doc Code:	SKI	T.Ph5b1.F03	reach	ing ribees.	5		Date:	07-08-20	019
ES × OA	MGALORE +	Title:	Сог	urse Lab Mai	nual				Page:	33 / 52	
Copyri	ght ©2017. c/	AS. All rights reserv	ed.			Data			Data		
-	Exper	iment No.:	1	Marks		Date	ч		Date Conducted		
1	Title		Code	Converters		Flaime	u		Jonducied	•	
2	Course	Outcomes	Desig	in and ana	lyze comb	inational c	ircuits l	ike add	ers, subtra	acters, p	oarity
			gene	rators and c	ode conver	ters using c	ombinat	ion of ga	ites	•	
3	Aim		To De	esign and im	plement co	de convert	er I)Bina	ry to Gra	y II) Gray to	Binary (Code
4	Matoria	/	using	basic gates)					
4	Fauipm	ient /	1.IC , 2 Dat	/404, IC/4 ch.chords	32, 10/408	5					
	Require	ed	3.Pov	ver chords							
			4.Tra	ainer Kit							
5	Theory,	Formula,	Binar	y to Gray							
	Principl	e, Concept	G3=B	3							
			GO=B	0⊕B1 1⊕B2							
			G2= E	1							
				J							
			Grey	to Binary							
			B3=G	3							
			B2=G	2 ⊕ G3							
			B1=G1	1 ⊕ G2 ⊕ G3	0.0						
6	Drocod		B0=0	i0 ⊕ G1⊕ G2 rifi (all aa	⊕G3		tolo olo		ula atla are t		
	Program	n. Activity.	I.vei	niy all co	mponents nor not	s anu pa	ich ch	ioras w	mether t	ney ar	e in
	Algorith	ım, Pseudo	yooc 2 Ma	ke connecti	TOF HOL.	n in the cire	ruit diad	ram			
	Code		3. Giv	e supply to	the trainer k	iit.	suit diag	ram.			
			4. Pro	vide input d	ata to the c	ircuit via sw	ritches.				
			5. Ver	rify truth tab	le sequence	e and obser	ve outp	ut			
7	Block,	Circuit,									
	Model	Diagram,		Bina	ry To Gray						
	Reactio	n Equation, ed Graph							Noute Disease		
		sa arapir	B0 <u>x1</u>						nay tu binary		- 🕢 вз
							G	3 📶		-	
					╗ᢕᡗ					5	- 🕢 в2
			BI XI		T_						
							G	2 1			
							31	Ē		L	
			B2 <u>x1</u>								- (1) B1
					4		G	1 🗐		-	
							2				
				2				Г		5	- ഹ B0
			B3 <u>x1</u>	┙╸	\sim	~				r''	
	Obcont	ation Table		Gra	y Code In	put	3 G Bir			ut	
	Look-u	auon rable, o Tahle		G3 (0	G2 G1	GO 0	B3	B2 0	B1 0	BO 0	
	Output			0	0 0 0 1	1	0	0	0	1	
				0	0 1	0	0	0	1 0	1 0	
				0	1 1 1 0	1	0	1	0	1	
				0	1 0	0	0	1	1	1	
CS			-	1	1 0	1	1	0	0	1	
Prep	bared by	/		1	1 1	0	1	0	1	1	ch
				1	0 1	1	1	1	0	1	
				1	0 0	1	1	1	1 1	1	

I

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SA CANGALORE *	Title:	Course Lab Manual	Page: 34 / 52

Copyr	ight ©2017. cAAS. All rights reserv	ed.
	Sample	
	Calculations	
10	Graphs, Outputs	Respective Truth tables are verified
11	Results & Analysis	
12	Application Areas	Code converters are used in data communication for error correction
13	Remarks	
14	Faculty Signature	
.	with Date	
L	1	1

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE *	Title:	Course Lab Manual	Page: 35 / 52

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SAWGALORE T	Title:	Course Lab Manual	Page: 36 / 52

<u>-</u>	Experiment No.:	1	Marks		Date Planned		Date Conducted	
1	Title	Parit	y Generator	and Parity C	hecker		conducted	
2	Course Outcomes							
3	Aim	То с	lesign and v	erify Truth	Table of 3-k	oit Parity Ge	enerator and	4-bit Parity
		Chec	ker using ba	sic Logic Gat	es with an ev	ven parity bi	t	-
4	Material /	1.IC	7404, IC743	32, IC7408				
	Required	2. Pa	tch chords					
		3.P0\ 4.Tra	iner Kit					
5	Theory, Formula	Thec	ory :Parity Ger	nerator and C	Checker A pa	rity generate	or is a combir	national logic
	Principle, Concept	circu that (it that genera checks the pa	ates the parit arity in the re	y bit in the tra ceiver is calle	ansmitter. O ed parity ch	n the other ha ecker.	and, a circuit
		The	sum of the d	ata bits and	parity bits ca	n be even c	or odd . In eve	en parity, the
		adde	parity the add	vill make the	e total numb will make th	er of 1s an e total num	even amoun ber of 1s odd	t wnereas in amount
		In ev	en parity bit s	scheme, the	parity bit is 'C)' if there are	even numbe	er of 1s in the
		data	stream and	the parity b	it is '1' if ther	re are odd i	number of 1s	in the data
		strea	m. In odd pa tho data stro	rity bit scher	ne, the parity	y bit is '1' if t)' if thoro ar	here are eve	n number of r of 1c in tho
		data	stream. Let u	is discuss bo	th even and	odd parity a	enerators.	
		3 bit	Parity Gener	ator Let us a	assume that	a 3-bit mes	sage is to be	transmitted
		with	an even paril	y bit. Let the	three inputs	A, B and C	are applied to	o the circuits
		and dene	output bit is	n parity hit F	OIT P. The TC D The figure	below show	of 1s must	be even, to able of even
		parit	y generator i	n which 1 is p	placed as par	rity bit in ord	der to make a	ill 1s as even
		wher	n the number	r of 1s in the t	ruth table is	odd.		
6	Procedure,	1. Ve	rify all compo	onents and p	atch chords	whether the	y are in good	condition or
	Program, Activity, Algorithm Pseudo	not. 2 Ma	ke connectic	ns as shown	in the circuit	t diagram		
	Code	3. Giv	e supply to t	he trainer kit		alagram.		
		4. Pro	ovide input da	ata to the cire	cuit via switcl	hes.		
		5. Ve	rify truth tabl	e sequence	and observe	outputs		
7	Block, Circuit, Model Diagram	Darity	Generator			Darity Cho	ckor	
	Reaction Equation		y denerator			Tanty One	chei	
	Expected Graph				— A			
					В	A-	\	
					— c	в		
							N.	~
		A	- In		P			
		B		Γ	2011			
			1.0000.000			cP	× .	
					- P	p	<u> </u>	
		C		ν	ā.			
	Observation Table	P	arity Generat	or		Parity Ch	ecker	
	Look-up Table		ancy denotat			i anty Off		
	Output							



SKIT	Teaching Process	Rev No.: 1.0
Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
Title:	Course Lab Manual	Page: 37 / 52

											_			
			3-bit message		Even parity	bit generator (P)		4-bi	t recei	ived mess	age	Parity er	ror check C	
							22		Α	B	C	Р		р
			Α	B	C		Y	_	0	0	0	0		0
			•	0	0		0		0	0	0	1		1
			U	U	U		0	-	0	0	1	0		1
			0	0	1		1	3	0	0	1	1		0
		-		•	•		•		0	1	0	1		0
			0	1	0		1	8	0	1	1			0
				N -	0	1			0	1	1	1		1
			0	1	1		0	5 -	1	0	0	0		1
			4	•	•		4		1	0	0	1		0
			1	U	U		1		1	0	1	0		0
			1	0	1		0		1	0	1	1		1
			1.				V		1	1	0	0		0
			1	1	0		0		1	1	0	1		1
							- C		1	1	1	0		1
			1	1	1		1		1	1	1	1		0
								~						
	Sample													
	Calculations													
10	Graphs Outputs	Resr	hect	ive T	ruth	tables	are verifie	-d						
10		1.001	0000		i atri	100100		Ju						
11	Results & Analysis													
12	Application Areas	Parit	v q	ener	ators	s and	checkers	are	used	in	error	detectio	n and	correctior
		tech	nia	les ir	n net	working	a systems	S						
12	Remarks						5 - 7	-						
10	Faculty Cignations													
14	Faculty Signature													
	with Date													

Logo	SKIT	Teaching Process	Rev No.: 1.0					
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019					
SA CANGALORE +	Title:	Course Lab Manual	Page: 38 / 52					
Copyright ©2017. cAAS. All rights reserved.								

SKIT					Rev No	0.: 1.0			
		Doc Code:	SKI	Г.Ph5b1.F03				Date:07	7-08-2019
S * BAN	GALORE	Title:	Cou	Course Lab Manual				Page: 3	9 / 52
Copyri	ght ©2017. c/	AS. All rights reserv	ed.					- 1	
-	Exper	iment No.:	8a	Marks		Date	D	ate	
1	Titlo		Macto		Flop	Planned	Cond	auctea	
2	Course	Outcomes	Doali7	e slave rlip	riup voressions u	sina multinla	vorIC		
2	∆im	Outcomes	Realiz		stor / Slavo	Flin-Flon us	ing NAND gates	and ve	rify its truth
5			table.				ing in ite gales		
4	Materia	l /	1 IC	74L S10					
	Equipm	ient	2 IC	741 500					
	Require	ed	2.10 2. Pa	tch chords					
			J. P∩ ⊿ P∩	wer chord					
			4. 1 U E Tra	ver eriora vinor kit	5				
5	Theory	Formula	5. 110 Tho 1	control inpu	its to a clo	cked flip fl	on will be mak	ina a t	ransition at
5	Principl	e. Concept	appro	ximately the	e same times	as triggering	edae of the cloc	:k input (occurs. This
		-,	can le	ad to unpre	dictable trigg	gering.	,		
			A JK r	master flip fl	op is positive	edge trigge	red, where as sla	ve is ne	gative edge
			trigge	red. Therefo	ore master firs	st responds t	o J and K inputs a	nd then	slave. If J=0
			and k	K=1, master	resets on ar	rival of posit	ive clock edge.	High ou	itput of the
			tha cl	ave is force	d to reset If	hoth the inr	uts are high it d	nandes i	the state or
			toaal	es on the ar	rival of the p	ositive clock	edae and the sl	ave too	ales on the
			negat	ive clock ed	ge. The slave	e does exactl	y what the maste	r does.	<u>.</u>
6	Proced	ure,	1.Ver	ify all co	mponents	and patch	chords whet	her th	ey are in
	Prograr	n, Activity,	good	l conditior	n or not.	·			
	Algorith	im, Pseudo	2. Mal	ke connectio	ons as shown	in the circuit	diagram.		
	Code		3. Give	e supply to t	he trainer kit.				
			4. Pro	vide input da	ata to the circ	cuit via switch	Ies.		
			5. ver	lly truth tabl	e sequence a	and observe	Sulpul		
7	Block.	Circuit.							
ĺ	Model	Diagram,							
	Reactio	n Equation,							1
	Expecte	ed Graph		1		<u>∖。</u> ⊥	9		
			J	13 7410	11 7410		7400 2 10 740	∘୵ᢪᠮᠮ	-• Q
				r d	\rightarrow		\rightarrow	<	
						>			
			к	0 4 7410	p6 2 12 7410	12 5	7400 01 12 740		• Q'
						/ 누리			
					3				
					4 5 7410) ⁶			
	Ohacii	otion Talal							
	Look-II	auon Table, n Table							
	Output								
				F	unction Tab	ole :			
				C	lock J K	<u>(0)</u>	Comment		
				F	ΠΟΟ	$0 0 0^{\circ}$	No Change		
					Π 0 1	$\frac{7}{0}$ $\frac{20}{1}$	Pasat		
					Π 0 1		C - t		
					$\frac{\Pi}{\Pi}$ 1 0	$\frac{1}{1}$	Set		
					11 1 1	$ \mathbf{Q}_0 \mathbf{Q}_0 $	Toggle		
1	1								

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
ANGALORE *	Title:	Course Lab Manual	Page: 40 / 52

	Sample Calculations	
10	Graphs, Outputs	Respective Truth tables are verified
11	Results & Analysis	
12	Application Areas	Flip flops are used in memory devices
13	Remarks	
14	Faculty Signature with Date	



SKIT	Teaching Process	Rev No.: 1.0
Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
Title:	Course Lab Manual	Page: 41 / 52

-	Experiment No.:	8b	Marks		Date Planned		Date Conducted			
1	Title	D Flip	-Flop with pa	ositive-edae	triaaerina.		conducted			
2	Course Outcomes	Desig trigge	Design and develop the Verilog / VHDL code for D Flip-Flop with positive-edge riggering. Simulate and verify its working.							
3	Aim	D Flip	-Flop with p	ositive-edge	triggering					
4	Material / Equipment Required	1. C	Desininging	software	tool					
5	Theory, Formula, Principle, Concept	It also is eith synch mostl 0, the Wher	t also has two outputs, with one being logically inverse of other. The data input s either logic 0 or 1, meaning low or high voltage. The clock input helps in synchronizing the circuit to an external signal. The set input and reset input are mostly held low. A D-type flip-flop can have two possible values. When input D = 0, the flip-flop undergoes a reset, which means the output would be set to 0.							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. 2. 3. 4. 5. Type	Create a n Create a n Create a n Enter the u Create a n the code as	ew project ew workshee ew blank pag user name ar ew VHDL son given	et ge Id input outp urce	ut variable d	letails			
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	<u> </u>								
	Observation Table, Look-up Table, Output									
	Sample Calculations									
10	Graphs, Outputs	Respe	ective Truth t	ables are ve	rified					
11	Results & Analysis									
12	Application Areas	Flip fl	ops are used	l in memory o	devices					
13	Remarks									
14	Faculty Signature with Date									

Logo	SKIT	Teaching Process	Rev No.: 1.0					
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019					
SA CANGALORE +	Title:	Course Lab Manual	Page: 42 / 52					
Copyright ©2017. cAAS. All rights reserved.								

	TUTE					– –							N.L.	_
150	-000	SKII			-00	Tea	cning i	Process	5			Rev	INO.: 1.0)
	500	Titlo		riigui.t	-∪3 Manur	al						Dale	0/-00 م: ۲۵ /	52 52 52
84M	GALORE		Cours		Manua	al						Fay	e. 43 /	54
-	Exper	iment No.:	ga	Mark	S		F	Date Plannee	ł		Co	Date nducte	∋d	
1	Title		Synchr	onous	counte	ər							•	
2	Course	Outcomes	Design	and a	nalyze	e syncl	nronou	is cou	nter a	nd as	ynchrc	nous (counte	rs using
			combir	nation c	of flip f	lops								
3	Aim		Design Flop IC	and in is and c	nplem 1emor	ent a r Istrate	nod-n its wor	(n<8) s king	synchr	onous	up co	ounter	using .	J-K Flip-
4	Materia	l /	1. IC 7	74LS76	6			0						
	Equipm	ent	2 10.7	1 508	3									
	Require	ed	2 Dot	2. IC /4LOUO										
					orda									
			4. 200											
	<u> </u>		5. Trai	ner Ki	ι								<u> </u>	
5	Theory, Principl	Formula e, Concept	The rip state. ⁻ where output The co count (and ge	he ripple counter requires a finite amount of time for each flip flop to change tate. This problem can be solved by using a synchronous parallel counter there every flip flop is triggered in synchronism with the clock and all the utput which are scheduled to change do so simultaneously. he counter progresses counting upwards in a natural binary sequence from ount 000 to count 100 advancing count with every negative clock transition and get back to 000 after this cycle.										
6	Procedu	Ire	1\/_rif		omn	nont	s and	natch	chor	de w	hothe	r tha	/ aro i	n aood
	Progran Algorith Code	n, Activity, ım, Pseudo	condi 2. Make 3. Give 4. Provi 5. Verif	tion or e conne supply ide inpu y truth	r not. ections to the ut data table s	s as sho e traine a to the sequer	own in r kit. e circui ice and	the circ t via sw d obser	cuit dia itches ve out	agram. .put				
7	Block	Circuit												
/	Model	Diagram	Circuit		- FM	- d 0 -								
	Reactio	n Equation	Circu	it diagra	m of M	od - 8 c	ounter:							
	Expecte	ed Graph												
		'			Vcc			1 QA		QB			000	
					_		U1A	1	U1B		muteros.		U2A	, ,
						_	2		7	1	U5A		2	
						4 J	PRE 15	9	PRE	11 2			e 15	
				Cloc	k Input	1 cL	ĸ	6 0	LK I		7408	1 CLK		
						16	= 14	12		10	Г	16 K	ō 14	
		3 8 8												
		Vcc												
	Observa Look-u	ation Table, o Table	DESI	GN FO	R MOI	D 8 UP	COUN	TER:						
	Output		Pr	esent St	ate	N	lext sta	te	12		Flip flo	p input	S	
			Qc	QB	QA	Q _{C+1}	Q _{B+1}	Q _{A+1}	Kc	J _C	K _B	JB	KA	J _A
			0	0	0	0	0	1	X	0	X	0	X	1
			0	0	1	0	1	0	X	0	X	1	1	X

Х

Х

X

X X

Х

X

Х

X

Х

X

Х

Х

Х

X

X

Х

X

3	000	SKIT	Teaching Process	Rev No.: 1.0
		Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
55 × 84	MGALORE +	Title:	Course Lab Manual	Page: 44 / 52
Copyri	ght ©2017. c/	AAS. All rights reserved	d.	
9	Sample	è		
	Coloulo	tions	Designs	

	Calculations	Design: JA KA	
		0 1 X X 1 0 X 1 1 X	
		1 1 X X 1 1 X 1 1 X	
		JA = 1 KA = 1	
		JB КВ	
		0 0 1 X X 0 X X 1 0	
		1 0 <u>1 X X</u> 1 0	
		JB = QA KB = QA	
10	Graphs, Outputs	Respective Truth tables are verified	
11	Results & Analysis		
12	Application Areas	Counters are used in digital clock	
13	Remarks		
14	Faculty Signature		
	with Date		

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SA ANGALORE T	Title:	Course Lab Manual	Page: 45 / 52
Copyright ©2017. cÅ	AS. All rights reserved		

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE *	Title:	Course Lab Manual	Page: 46 / 52
Construction to the Construction of the Constr	A C All of eleka to a store of		

Copyri	ght ©2017. cAAS. All rights reserv	red.							
-	Experiment No.:	9b	Marks		Date Planned		Date Conducted		
1	Title	mod	d-8 up count	er					
2	Course Outcomes	Desig and \	gn and deve verify its worl	lop the Veril king	og / VHDL o	code for mo	d-8 up coun	ter. Simulate	
3	Aim	VHD	code for m	od-8 up cou	nter				
	Material /	1	Designing	software to					
4	Equipment Required	1.	Designing						
5	Theory, Formula Principle, Concept	Then, sequ signa coun calle numl	counters a ence of cou Il. The numb ter advances d the modul per of states	are sequent nting states er of states o s before retu us (MOD). In the counter o	ial logic de which are t or counting s urning once a other words counts and is	vices that f riggered by equences th again back t , the modulu the dividing	follow a pre an external nrough which o its original us (or just m number of t	edetermined clock (CLK) a particular first state is odulo) is the he counter.	
6	Procedure,	1	. Create a r	new project					
	Program, Activity,	2	. Create a r	new workshe	et				
	Algorithm, Pseudo	3	. Create a r	new blank pa	ge				
	Code	4	. Enter the	user name a	nd input outp	out variable o	details		
		5	. Create a r	new VHDL sc	ource				
		Туре	the code as	given					
7	Block, Circuit			_					
	Model Diagram Reaction Equation Expected Graph								
	Observation Table				D 187 WE DD waards file		1.*		
	Look-up Table	Signal nan	ne Value	400	800	1200	1600 2	000 2400	
		Inpu	S	and the second second			Inputs	a da a a a a a	
	Oulpul	₽- Clk							
		► rese	t	0					
		Outp	uts				Outputs		
		E - dout		201123	X4X5X0X1X2	3 7 4 7 5 7 0 7 1 7	2 73 0 7 1 7 2 7	3 7 4 7 5 7 0 7 1 7	
			out[2]						
			out[1]	1					
		-0 0							
		-0 0	out[0]						
9	Sample								
Ĭ	Calculations								
10	Graphs, Outputs	Resp	ective Truth	tables are ve	rified				
11	Doculto 8 Apolycia								
11	Results & Analysis								
<u> </u>		0							
12	Application Areas	Cour	iters are used	d in digital cl	ock				
13	Remarks								
14	Faculty Signature	,							
	with Date								

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SA ANGALORE T	Title:	Course Lab Manual	Page: 47 / 52
Copyright ©2017. cÅ	AS. All rights reserved		

STATE OF	OGO.	SKIT			Teaching Process	ng Process		Rev No.: 1.0	
		Doc Code:	SKI	Г.Ph5b1.F03			Date:07-08-2019		
SS * BAN	GALORE	Title:	Cou	irse Lab Manua	Page: 48 / 52				
Copyrig	ght ©2017. cÅ	AS. All rights reserve	ed.						
-	Exper	iment No.:	10	Marks	Date Planned	Da Cond	ate lucted		
1	Title		Async	chronous coun	ter				
_	<u> </u>	<u> </u>	D						

2	Course Outcomes	Design and	a analyze n of flip fl	synchror	ious count	er and asynch	ronous counters using		
3	Aim	Design and	l implem	ent an as	vnchronous	counter using	decade counter IC to		
5		count up fr	rom 0 to	n(n<=9) ai	nd demonst	rate on 7-segr	ment display (using IC-		
		7447).							
4	Material /	1.IC7490,	IC7443						
	Equipment	2. Patch cho	ords						
	Requirea	3.Power ch	ords						
		4.Trainer Ki	t						
5	Theory, Formula, Principle, Concept	Asynchrono clock input flop is trig introduces input clock exactly at t triggered, v	synchronous counter is a counter in which the clock signal is connected to the ock input of only first stage flip flop. The clock input of the second stage flip p is triggered by the output of the first stage flip flop and so on. This troduces an inherent propagation delay time through a flip flop. A transition of put clock pulse and a transition of the output of a flip flop can never occur kactly at the same time. Therefore, the two flip flops are never simultaneously iggered, which results in asynchronous counter operation.						
6	Procedure,	1Verify all	compo	pnents ar	nd patch c	hords wheth	her they are in good		
	Program, Activity,	condition	or not						
	Algorithm, Pseudo	2 Make cor	inections	as shown	in the circui	t diagram			
	Code	3. Give supr	oly to the	trainer kit		e alagiani.			
		4. Provide ir	nput data	to the circ	cuit via switc	hes.			
		5. Verify tru	th table s	equence	and observe	output			
	Model Diagram, Reaction Equation, Expected Graph	odel Diagram, eaction Equation, cpected Graph							
8	Observation Table,								
	Output	Clack	•	D	C				
		CLOCK	A	В					
		0	0	0	0	0			
		1	0	0	0	1			
		2	0	0	1	0	-		
		3	0	0	1	1	-		
		4	0	1	0	0	-		
		5	0	1	0	1	-		
		6	0	1	1	0			

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE +	Title:	Course Lab Manual	Page: 49 / 52
Copyright ©2017. c/	AAS. All rights reserve	1.	·

		7	1	0	0	0	
		8	1	0	0	1	
9	Sample Calculations						
10	Graphs, Outputs	Respective	Truth tak	oles are ve	rified		
11	Results & Analysis						
12	Application Areas	Counters ar	e used in	digital clo	ck		
13	Remarks						
14	Faculty Signature with Date						

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
ANGALORE *	Title:	Course Lab Manual	Page: 50 / 52

Logo		SKIT		Teaching Process					0.: 1.0
		Doc Code:	SKI	T.Ph5b1.F03	Date:C	7-08-2019			
		Title:	Col	ırse Lab Mar	nual			Page:	51 / 52
Copyrie	ght ©2017. c/	AS. All rights reserv	ed.						
-	Exper	iment No.:	10	Marks		Date Planned		Date Conducted	
1	Title		Digita	I to analog c	converter		I		
2	Course	Outcomes	Gene	rate ramp wa	aveform by E	DAC using co	unter IC		
3	Aim		Gene	rate a Ramp	output way	eform using	DACo8oo (II	nputs are g	iven to DAC
	through IC74393 dual 4-bit binary counter).								
4	Material / Equipment Required		DAC0800, IC74393, Trainer Kit, Patch chords , CRO						
5	Theory, Principl	Formula, e, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code		 Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe outpu 						
7	Block, Model Reactio Expecte	Circuit, Diagram, n Equation, ed Graph			5k 5k 5k 14 5k 15 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		Vout	• TO 20 Vp-p
8	Observ Look-u Output	ation Table, p Table,							
9	Sample Calcula	tions							
10	Graphs	Outputs		00	он			FFH	
11	Results	& Analysis							
12	Applica	tion Areas	DAC a	are used in d	lata transmis	sion			
12	Remark	(S							
1/	Faculty	Signature							
-4	with Da	te							
L									

Logo	SKIT	Teaching Process	Rev No.: 1.0
	Doc Code:	SKIT.Ph5b1.F03	Date:07-08-2019
SANGALORE *	Title:	Course Lab Manual	Page: 52 / 52