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Note : Remove “Table of Content” before including in CP Book

18CSL37 : ANALOG AND DIGITAL ELECTRONICS LAB

A. LABORATORY INFORMATION

1. Lab Overview

Degree:	BE	*Program:*	CS
Year / Semester :	2 / 3	*Academic Year:*	2018-19
Course Title:	Analog and Digital Electronics Lab	*Course Code:*	18CSL37
Credit / L-T-P:	2 / 1-0-2	*SEE Duration:*	180 Minutes
Total Contact Hours:	40 Hrs	*SEE Marks:*	60Marks
CIA Marks:	40	*Assignment*	1 / Module
Course Plan Author:	Prof. Geetha Megaraj/Rashmi K T	*Sign*	Dt :
Checked By:		*Sign*	Dt :

2. Lab Content

Unit	Title of the Experiments	Lab Hours	Concept	Blooms Level
1	a) Design and construct a Schmitt trigger using Op-Amp for given UTP and LTP values and demonstrate its working. b) Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working.	03	Analog Circuit Design	L4 Analyze
2	a) Design and construct a rectangular waveform generator (Op-Amp relaxation oscillator) for given frequency and demonstrate its working. b) Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and demonstrate the change in frequency when all resistor values are doubled.	03	Analog Circuit Design	L4 Analyze
3	Design and implement an Astable multivibrator circuit using 555 timer for a given frequency and duty cycle.	03	Analog Circuit Design	L4 Analyze
4	Design and implement Half adder, Full Adder, Half Subtractor, Full Subtractor using basic gates.	03	Combinational circuit design	L4 Analyze
5	a) Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC. b) Design and develop the Verilog /VHDL code for an 8:1 multiplexer. Simulate and verify its working.	03	Boolean expression realization	L4 Analyze
6	Design and implement code converter I)Binary to Gray (II) Gray to Binary Code using basic gates.	03	Code converters design	L4 Analyze
7	Design and verify the Truth Table of 3-bit Parity Generator and 4-bit Parity Checker using basic Logic Gates with an even parity bit.	03	Parity generator and Checker design	L4 Analyze
8	a) Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table. b) Design and develop the Verilog / VHDL code for D Flip-Flop with positive edge triggering. Simulate and verify it's working.	03	JK Master/ Slave flip flop realization	L3 Analyze
9	a) Design and implement a mod-n (n<8) synchronous up counter using J-K Flip- Flop ICs and demonstrate its working. b) Design and develop the Verilog / VHDL code for mod-8 up counter. Simulate and verify it's working.	03	counter design	L4 Analyze
10	Design and implement an asynchronous counter using decade counter IC to count up from 0 to n (n<=9) and demonstrate on 7-segment display (using IC- 7447).	03	counter design	L4 Analyze
11	Generate a Ramp output waveform using DAC0800 (Inputs are given to DAC through IC74393 dual 4-bit binary counter).	03	DAC realization	L4 Analyze

3. Lab Material

Unit	Details	Available
1	Text books	
		In Lib
2	Reference books	
		In dept
3	Others (Web, Video, Simulation, Notes etc.)	
		Not Available

4. Lab Prerequisites:

-	-	Base Course:		-	-
SNo	Course Code	Course Name	Topic / Description	Sem	Remarks
1	15CSL37	Analog and Digital Electronics Lab	Knowledge on basic gates.	2	
			Knowledge on Boolean expressions	2	

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

5. General Instructions

SNo	Instructions	Remarks
1	Observation book and Lab record are compulsory.	
2	Students should report to the concerned lab as per the time table.	
3	After completion of the program, certification of the concerned staff in-charge in the observation book is necessary.	
4	Student should bring a notebook of 100 pages and should enter the readings /observations into the notebook while performing the experiment.	
5	The record of observations along with the detailed experimental procedure of the experiment in the Immediate last session should be submitted and certified staff member in-charge.	
6	Should attempt all problems / assignments given in the list session wise.	
7	It is responsibility to create a separate directory to store all the programs, so that nobody else can read or copy.	
8	When the experiment is completed, should disconnect the setup made by them, and should return all the components/instruments taken for the purpose.	
9	Any damage of the equipment or burn-out components will be viewed seriously either by putting penalty or by dismissing the total group of students from the lab for the semester/year	
10	Completed lab assignments should be submitted in the form of a Lab Record in which you have to write the algorithm, program code along with comments and output for various inputs given	

6. Lab Specific Instructions

SNo	Specific Instructions	Remarks
1	Verify all the components and patch cords for their good working condition	
2	Make connections as shown in the circuit diagram	
3	Give supply to the trainer kit	
4	Provide input data to the circuit via switches and verify the truth table for digital experiments	
5	Verify the output waveform on Cathode Ray Oscilloscope	

B. OBE PARAMETERS

1. Lab / Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
1	Design and analyze circuits schmitt trigger and rectangular waveform generator using operation amplifier IC and 555 IC	09	Analog Circuit Design	Instructions & Demonstration	Slip Test	L4
2	Design and analyze combinational circuits like adders, subtracters, parity generators and code converters using combination of gates	09	Combinational circuit design	Instructions & Demonstration	Slip Test	L4
3	Realize boolean expressions using multiplexer IC	03	Boolean expression realization	Instructions & Demonstration	Slip Test	L4
4	Realize JK master slave flip flop using nand gates	03	JK Master/ Slave flip flop realization	Instructions & Demonstration	Slip Test	L4
5	Design and analyze synchronous counter and asynchronous counters using combination of flip flops	03	Counter deign	Instructions & Demonstration	Slip Test CIA	L4
6	Generate ramp waveform by DAC using counter IC	03	DAC realization	Instructions & Demonstration	Slip Test CIA	L4
7	Understand simulation toolkit to design analog circuits	03	Analog Circuit simulation	Instructions & Demonstration	Slip Test CIA	L4
8	Understand simulation toolkit to design digital circuits	06	Digital Circuit simulation	Instructions & Demonstration	Assignment	L4
10						
11						
-	**Total**	**42**	-	-	-	-

Note: Identify a max of 2 Concepts per unit. Write 1 CO per concept.

2. Lab Applications

SNo	Application Area	CO	Level
1	Waveform generators are used in signal generators	CO1	L4
2	Adders are used in Arithmetic logic unit	CO2	L4
3	Multiplexers are used in communication systems	CO3	L2
4	Flip flops are used in memory devices	CO4	L4
5	Counters are used in Digital clock	CO5	L4
6	Digital to analog converters are used in data transmission	CO6	L4
7	Simulation toolkits are used to design and test circuits	CO7,CO8	L3

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	Level
CS501PC.1	Design and analyze circuits schmitt trigger and rectangular waveform generator using operation amplifier IC and 555 IC	2	2											L2
CS501PC.2	Design and analyze combinational circuits like adders, subtracters, parity generators and code converters using combination of gates	3	3											L2
CS501PC.3	Realize boolean expressions using multiplexer IC	2												L2
CS501PC.4	Realize JK master slave flip flop using nand gates	2	3											L3
CS501PC.5	Design and analyze synchronous counter and asynchronous counters using combination of flip flops	3												L2
CS501PC.6	Generate ramp waveform by DAC using counter IC		1											L2
CS501PC.7	Understand simulation toolkit to design analog circuits					2								L3
CS501PC.8	Understand simulation toolkit to design digital circuits					2								L2

Note: Mention the mapping strength as 1, 2, or 3

4. Mapping Justification

Mapping		Mapping Level	Justification
CO	**PO**	**-**	**-**
CO1	PO1	2	Knowledge is required in construction of amplifiers and receivers
CO1	PO2	2	Analysis of amplifier and receiver circuits knowledge is required
CO2	PO1	3	Knowledge of adders and subtracters is required in design of ALU. Parity generators and code converters in communication systems
CO2	PO2	3	Adders and subtracters used to analyze ALU. Parity generators and code converters used to analyze communication systems
CO3	PO1	2	Knowledge is required in design of simplified circuits using multiplexer
CO4	PO1	2	Knowledge is required to build memory devices
CO4	PO2	3	To analyze memory devices flip flops are used
CO4	PO3	3	flip flops are used to design memory devices
CO5	PO1	3	Knowledge of counters helps the student to build timers and digital clocks
CO5	PO2	3	counters knowledge is required to analyze timers and digital clocks
CO5	PO3	2	counters are used to design timers and digital clocks
CO6	PO2	1	Knowledge is required to analyze working of communication systems
CO7	PO5	2	Use of simulation toolkit required to understand actual working of analog circuits
CO8	PO5	2	Use of simulation toolkit required to understand actual working of digital circuits

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					

Note: Anything not covered above is included here.

C. COURSE ASSESSMENT

1. Course Coverage

Unit	Title	Teaching Hours	No. of question in Exam							CO	Levels
			CIA-1	CIA-2	CIA-3	Asg-1	Asg-2	Asg-3	SEE		
1	Schmitt Trigger	05	1	-	-	-	-	-	1	CO1	L4
2	Rectangular Waveform Generator	05	1	-	-	-	-	-	1	CO1	L4
3	Astable Multivibrator	03	1	-	-	-	-	-	1	CO1	L4
4	Full adder, Full Subtractor	03	-	1	-	-	-	-	1	CO2	L4
5	Multiplexer	05	-	1	-	-	-	-	1	CO3	L4
6	Binary to Gray	03	-	1	-	-	-	-	1	CO2	L4
7	Parity Generator and Checker	03	-	1	-	-	-	-	1	CO2	L4
8	JK Master slave Flip flop	05	-	-	1	-	-	-	1	CO4	L4
9	Synchronous Counter	05	-	-	1	-	-	-	1	CO5	L4
10	Asynchronous counter	03	-	-	1	-	-	-	1	CO5	L4
11	DAC0800	03	-	-	1	-	-	-	1	CO6	L4
-	**Total**	**60**	**7**	**8**	**5**	**5**	**5**	**5**	**20**	**-**	**-**

Note: Write CO based on the theory course.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	25		
CIA Exam – 2			
CIA Exam – 3			
record	15		
Final CIA Marks	**40**	**-**	**-**

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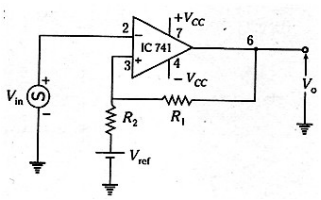
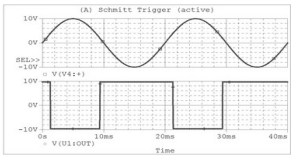
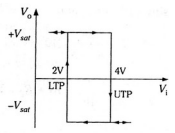
SNo	Description	Marks
1	Observation and Weekly Laboratory Activities	05 Marks
2	Record Writing	10 Marks for each Expt
3	Internal Exam Assessment	25 Marks
4	Internal Assessment	40 Marks
5	SEE	60 Marks
-	**Total**	**100 Marks**

D. EXPERIMENTS

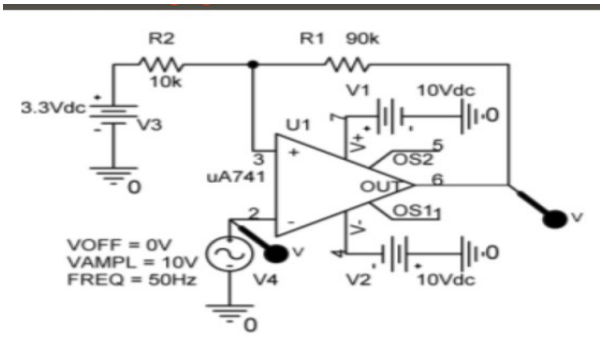
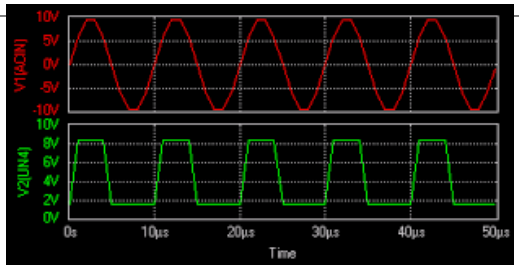
Experiment 01 :

-	**Experiment No.:**	1a	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Schmitt Trigger						
2	Course Outcomes	Design and analyze circuits schmitt trigger and rectangular waveform generator using operation amplifier IC and 555 IC						
3	Aim	Design and implement the Schmitt Trigger using µA741 Op-Amp or given UTP and LTP values.						
4	Material / Equipment Required	Opamp,Resistors,DC regulated power supply,Dual power DC power supply Signal generator,CRO,Connecting wires,CRO probes,Bread Board						
5	Theory, Formula, Principle, Concept	DESIGN From theory of Schmitt trigger circuit using op-amp, we have the triggering points, UTP= $\frac{R1Vref}{R1+R2}+\frac{R2Vsat}{r1+r2}$ Vsat is positive saturation of the opamp =90% of VCC LTP = $\frac{R1Vref}{R1+R2}-\frac{R2Vsat}{r1+r2}$ Hence given the LTP & UTP values to find the values R1,R2 and Vref values, the following design is used. UTP + LTP = $\frac{2R1Vref}{R1+R2}$------(1) UTP – LTP = $\frac{2R1Vsat}{R1+R2}$ ------(2) Let Vsat = 10V, UTP = 4V & LTP = 2V, then equation (2) yields R1=9R2 R2= 10 KΩ R1=90 KΩ (UTP + LTP) + From equation (1) we have Vref=$\frac{((UTP+LTP)(R1+R2))}{2R1}$=3.33 V						
6	Procedure, Program, Activity, Algorithm, Pseudo Code1	1)Connect the circuit as shown the diagram. 2)Set +Vcc and -Vcc to +12V and -12V respectively 3)Set Vref as per the design. 4)Apply Vin a sinusoidal signal of frequency around 500Hz 10Vpp from the signal generator. 5)observe the Input and output waveforms on the CRO 6)Using XY mode observe the hysteresis curve.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							

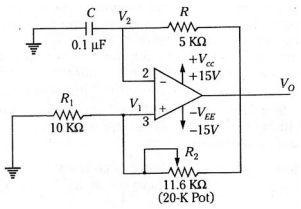
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	  Designed value of UTP = 4V Designed value of LTP = 2V Designed value of Hysteresis = 2 V (UTP – LTP)
11	Results & Analysis	
12	Application Areas	Waveform generators are used in signal generators
13	Remarks	
14	Faculty Signature with Date	

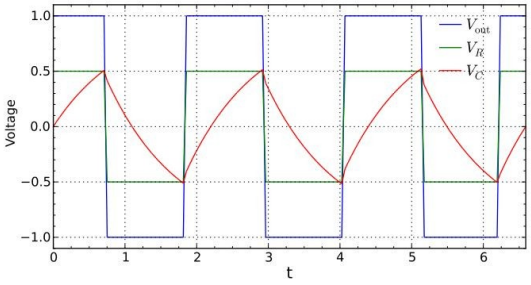
Experiment 01 :

-	**Experiment No.:**	1b	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Schmitt Trigger						
2	Course Outcomes	Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working.						
3	Aim	Design and implement a Schmitt trigger using Op-Amp using a simulation package for two sets of UTP and LTP values and demonstrate its working.						
4	Material / Equipment Required	1. uA 741 2. resistors 10k, 90k 3. vdc 3.3 , 10 4. voltages 5. ground '0' source 6. designing software						
5	Theory, Formula, Principle, Concept	DESIGN From theory of Schmitt trigger circuit using op-amp, we have the triggering points, UTP= $\frac{R1Vref}{R1+R2}+\frac{R2Vsat}{r1+r2}$ Vsat is positive saturation of the opamp =90% of VCC LTP = $\frac{R1Vref}{R1+R2}-\frac{R2Vsat}{r1+r2}$ Hence given the LTP & UTP values to find the values R1,R2 and Vref values, the following design is used. UTP + LTP = $\frac{2R1Vref}{R1+R2}$------(1) UTP – LTP = $\frac{2R1Vsat}{R1+R2}$ ------(2) Let Vsat = 10V, UTP = 4V & LTP = 2V, then equation (2) yields R1=9R2 R2= 10 KΩ R1=90 KΩ (UTP + LTP) + From equation (1) we have Vref=$\frac{((UTP+LTP)(R1+R2))}{2R1}$=3.33 V						
6	Procedure, Program, Activity, Algorithm, Pseudo Code1	1. design the circuit as shown the diagram. 2. Set vdc values and resistor values 3. connect 0 source ground connection 4. place the wires and design as per given in circuits 5. set Run to time: 40msec 6. set step size:0.1msec 7. run the project design to get the expected waveform.						

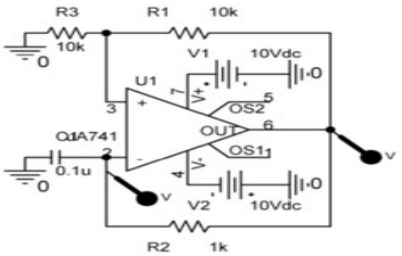
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	
8	Observation Table, Look-up Table, Output	
9	Sample Calculations	
10	Graphs, Outputs	 Designed value of UTP = 4V Designed value of LTP = 2V Designed value of Hysteresis = 2 V (UTP – LTP)
11	Results & Analysis	
12	Application Areas	Waveform generators are used in signal generators
13	Remarks	
14	Faculty Signature with Date	

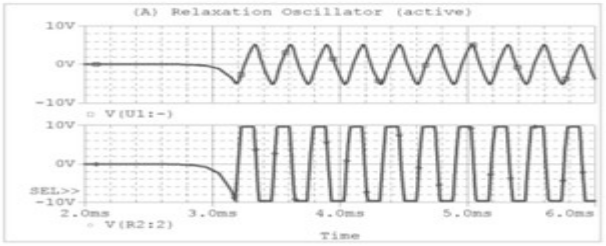
Experiment 02 :

-	**Experiment No.:**	2	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Rectangular waveform generator (Op-Amp relaxation oscillator)						
2	Course Outcomes	Design and analyze circuits Schmitt trigger and rectangular waveform generator using operation amplifier IC and 555 IC						
3	Aim	To design and implement the rectangular waveform generator (Op-Amp relaxation oscillator) for given frequency						
4	Material / Equipment Required	Opamp,Resistors,Capacitors,Dual power DC power supply, CRO, Connecting wires,CRO probes,Bread Board						
5	Theory, Formula, Principle, Concept	The period of the output rectangular wave is given as T$2RC\,ln\frac{1+B}{1-B}$-----(1) Where, B= $\frac{R1}{R1+R2}$ is the feedback fraction If R 1 = R 2 , then from equation (1) we have T = 2RC ln(3) Another example, if R 2 =1.16 R 1 , then T = 2RC ----------(2) Example: Design for a frequency of 1kHz (implies T= 1/f = 1/10^{3} = 10^{-3} = 1ms Use R 2 =1.16 R 1, for equation (2) to be applied. Let R 1 = 10kΩ, then R 2 = 11.6kΩ (use 20kΩ potentiometer as shown in circuit figure) Choose next a value of C and then calculate value of R from equation (2). Let C=0.1μF (i.e., 10 -7), then R= T/2C = $\frac{10}{2*10}$=5KΩ The voltage across the capacitor has a peak voltage of $\frac{R1}{R1+R2}$Vsat						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Connect the circuit as shown the diagram. 2. Set +Vcc and -Vcc to +12V and -12V respectively 3. observe the output waveforms on the CRO 4. Note down the Period T on the time scale on the CRO and hence compute the Frequency.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output							
9	Sample Calculations							

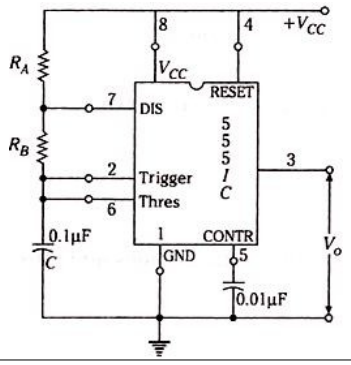
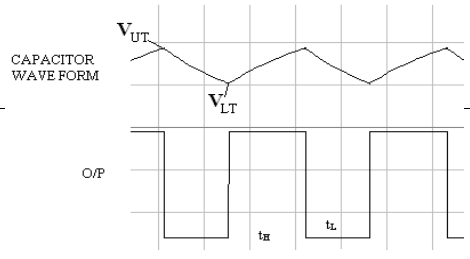
10	Graphs, Outputs	
11	Results & Analysis	
12	Application Areas	
		Waveform generators are used in signal generators
13	Remarks	
14	Faculty Signature with Date	

Experiment 02 :

-	**Experiment No.:**	2b	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Rectangular waveform generator (Op-Amp relaxation oscillator)						
2	Course Outcomes	Design and implement a rectangular waveform generator (Op-Amp relaxation oscillator) using a simulation package and demonstrate the change in frequency when all resistor values are doubled.						
3	Aim	To design and implement the rectangular waveform generator (Op-Amp relaxation oscillator) for given frequency						
4	Material / Equipment Required	1. uA 741 2. resistors 10k, 10k 3. vdc 3.3 , 10 4. voltages 5. ground '0' source 6. Capacitor 0.1 6. designing software						
5	Theory, Formula, Principle, Concept	The period of the output rectangular wave is given as T$2\,RC\,ln\frac{1+B}{1-B}$-----(1) Where, B= $\frac{R1}{R1+R2}$ is the feedback fraction If R 1 = R 2 , then from equation (1) we have T = 2RC ln(3) Another example, if R 2 =1.16 R 1 , then T = 2RC ----------(2) Example: Design for a frequency of 1kHz (implies T= 1/f = 1/10^{3} = 10^{-3} = 1ms Use R 2 =1.16 R 1, for equation (2) to be applied. Let R 1 = 10kΩ, then R 2 = 11.6kΩ (use 20kΩ potentiometer as shown in circuit figure) Choose next a value of C and then calculate value of R from equation (2). Let C=0.1μF (i.e., 10 -7), then R= T/2C = $\frac{10}{2*10}$=5KΩ The voltage across the capacitor has a peak voltage of $\frac{R1}{R1+R2}$Vsat						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Connect the circuit as shown the diagram. 2. Set +Vcc and -Vcc to +12V and -12V respectively 3. observe the output waveforms on the CRO 4. Note down the Period T on the time scale on the CRO and hence compute the Frequency.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output							
9	Sample Calculations							

10	Graphs, Outputs	
11	Results & Analysis	
12	Application Areas	Waveform generators are used in signal generators
13	Remarks	
14	Faculty Signature with Date	

Experiment 03 :

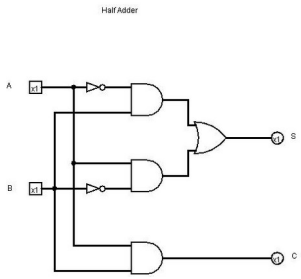
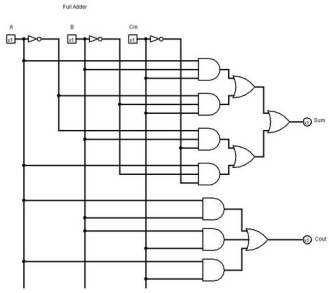
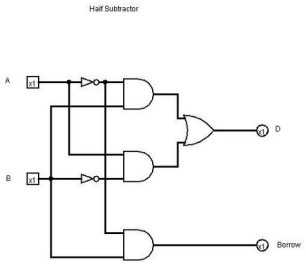
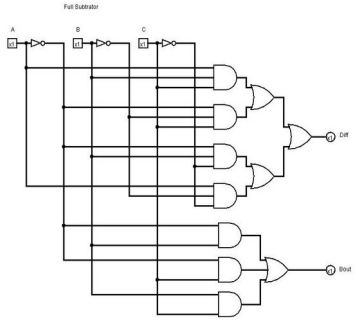
-	**Experiment No.:**	1	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	555 Timer						
2	Course Outcomes	Design and analyze circuits schmitt trigger and rectangular waveform generator using operation amplifier IC and 555 IC						
3	Aim	To design and implement the rectangular waveform generator (Op-Amp relaxation oscillator) for given frequency						
4	Material / Equipment Required	Timer IC 555,Resistors,Capacitor,DC regulated power supply,Signal generator & CRO,Connecting wires,CRO probes, Bread Board						
5	Theory, Formula, Principle, Concept	DESIGN Given frequency (f) = 1KHz and duty cycle = 60% (=0.6) The time period T =1/f = 1ms = t H + t L Where t H is the time the output is high and t L is the time the output is low. From the theory of Astable multivibrator using 555 Timer, we have t H = 0.693 R B C --------(1) t L = 0.693 (R A + R B)C ------(2) T = t H + t L = 0.693 (R A +2 R B) C Duty cycle = t H / T = 0.6. Hence t H = 0.6T = 0.6ms and t L = T – t H = 0.4ms. Let C=0.1μF and substituting in the above equations, R B = 5.8KΩ (from equation 1) and R A = 2.9KΩ (from equation 2 & R B values). The Vcc determines the upper and lower threshold voltages (observed from the capacitor voltage waveform) as UT = CC ∧ LT = CC . Note: The duty cycle determined by R A & R B can vary only between 50 & 100%. If R A is much smaller than R B , the duty cycle approaches 50%. Example 2: frequency = 1kHz and duty cycle =75%, R A = 7.2kΩ & R B =3.6kΩ, choose R A = 6.8kΩ and R B = 3.3kΩ.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Connect the circuit as shown the diagram. 2. Set +Vcc to +5V 3. observe the output waveforms on the CRO 4. Note down the Period Ton and Toff on the time scale on the CRO and hence compute the period T and Frequency f. 5. Compute the duty cycle.						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output							
9	Sample Calculations							
10	Graphs, Outputs							

CS
Prepared by

Approved. Patch

11	Results & Analysis	
12	Application Areas	Waveform generators are used in signal generators
13	Remarks	
14	Faculty Signature with Date	

Experiment 04 : .....

-	**Experiment No.:**	1	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Adders and Subtracters						
2	Course Outcomes	Design and analyze combinational circuits like adders, subtracters, parity generators and code converters using combination of gates						
3	Aim	To Design and implement Half adder, Full Adder, Half Subtractor, Full Subtractor using basic gates.						
4	Material / Equipment Required	1.C 7404, IC7432, IC7408 2. Patch chords 3.Power chords 4.Trainer Kit						
5	Theory, Formula, Principle, Concept	Application Areas						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe output						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	Half Adder  full adder  half subtracter full subtracter   						
8	Observation Table, Look-up Table, Output							

A	B	Sum	Carry
0	0	0	0

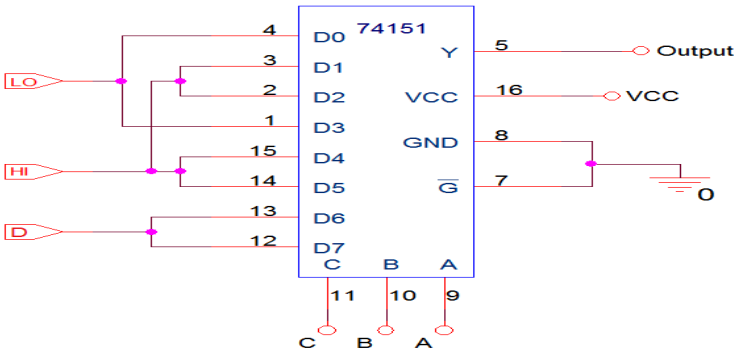
A	B	C	D	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Inputs		Outputs	
A	B	D_i(Difference)	B_o(Borrow)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

9	Sample Calculations	
10	Graphs, Outputs	Respective Truth tables are verified
11	Results & Analysis	
12	Application Areas	Adders and subtracters are used in arithmetic logic unit
13	Remarks	
14	Faculty Signature with Date	

Expt 5

-	**Experiment No.:**	5a	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Multiplexer						
2	Course Outcomes	Design and analyze combinational circuits like adders, subtracters, parity generators and code converters using combination of gates						
3	Aim	Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC.						
4	Material / Equipment Required	1 IC 74LS151 2. Patch chords 3.Power chords 4.Trainer Kit						
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe output						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output							
9	Sample Calculations							
10	Graphs, Outputs	Respective Truth tables are verified						

Decimal	A	B	C	D	f	MEV map entry
0	0	0	0	0	0	0 □D0
1	0	0	0	1	0	
2	0	0	1	0	1	1 □D1
3	0	0	1	1	1	
4	0	1	0	0	1	1 □D2
5	0	1	0	1	1	
6	0	1	1	0	0	0 □D3
7	0	1	1	1	0	
8	1	0	0	0	X	X □D4
9	1	0	0	1	X	
10	1	0	1	0	X	X □D5
11	1	0	1	1	X	
12	1	1	0	0	0	D □D6
13	1	1	0	1	1	
14	1	1	1	0	0	D □D7
15	1	1	1	1	1	

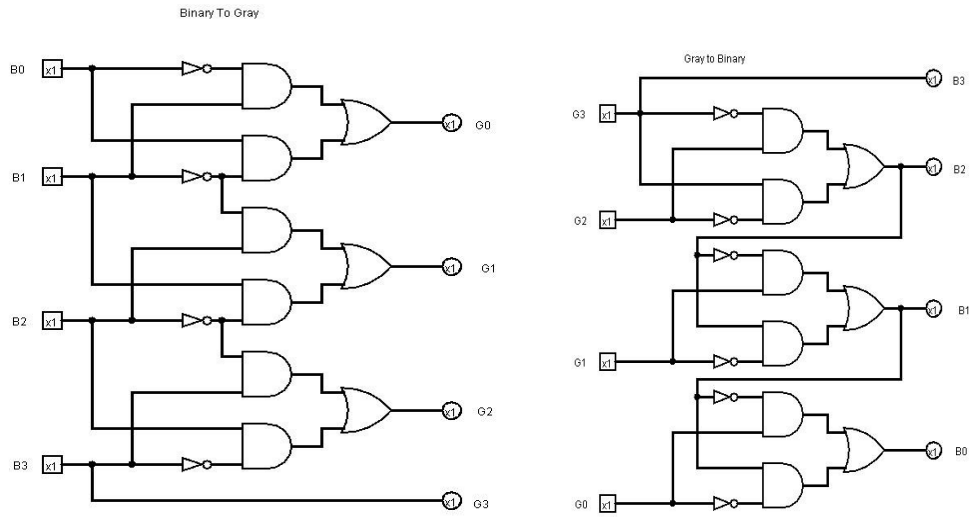
11	Results & Analysis	
12	Application Areas	Adders and subtracters are used in arithmetic logic unit
13	Remarks	
14	Faculty Signature with Date	

Expt 5

-	**Experiment No.:**	5b	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Multiplexer						
2	Course Outcomes	Design and develop the Verilog /VHDL code for an 8:1 multiplexer. Simulate and verify its working						
3	Aim	Verilog /VHDL code for an 8:1 multiplexer						
4	Material / Equipment Required	1. Designing tool software						
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Create a new project 2. Create a new worksheet 3. Create a new blank page 4. Enter the user name and input output variable details 5. Create a new VHDL source 6. Type the code as given						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output							
9	Sample Calculations							
10	Graphs, Outputs	Respective Truth tables are verified						
11	Results & Analysis							
12	Application Areas	Adders and subtracters are used in arithmetic logic unit						
13	Remarks							
14	Faculty Signature with Date							

Expt 6

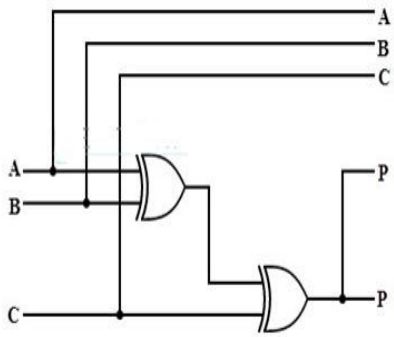
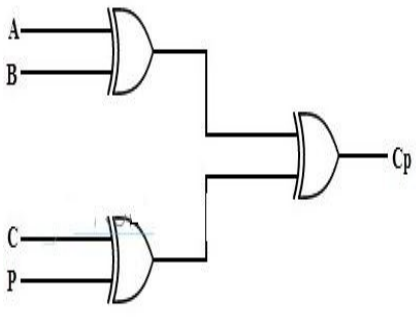
-	**Experiment No.:**	1	**Marks**		**Date Planned**		**Date Conducted**	

1	Title	Code Converters
2	Course Outcomes	Design and analyze combinational circuits like adders, subtracters, parity generators and code converters using combination of gates
3	Aim	To Design and implement code converter I)Binary to Gray II) Gray to Binary Code using basic gates.
4	Material / Equipment Required	1.IC 7404, IC7432, IC7408 2. Patch chords 3.Power chords 4.Trainer Kit
5	Theory, Formula, Principle, Concept	Binary to Gray G3=B3 G0=B0 ⊕ B1 G1=B1 ⊕ B2 G2= B2 ⊕ B3 Grey to Binary B3=G3 B2=G2 ⊕ G3 B1=G1 ⊕ G2 ⊕ G3 B0= G0 ⊕ G1⊕ G2 ⊕ G3
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe output
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	
	Observation Table, Look-up Table, Output	

Gray Code Input				Binary Code Output			
G3	G2	G1	G0	B3	B2	B1	B0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

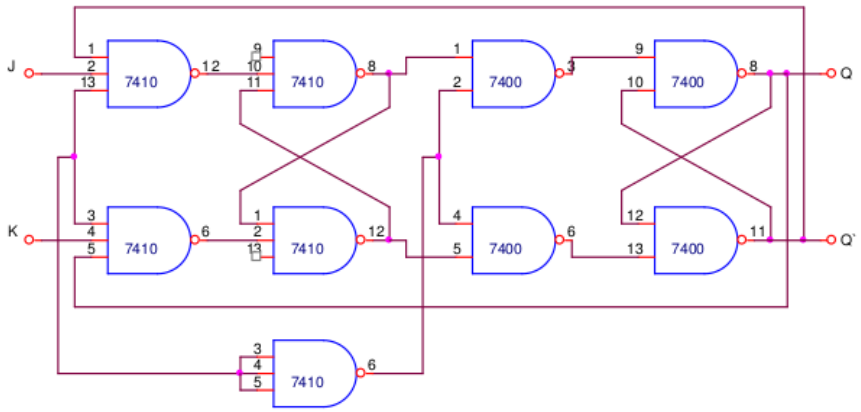
	Sample Calculations	
10	Graphs, Outputs	Respective Truth tables are verified
11	Results & Analysis	
12	Application Areas	Code converters are used in data communication for error correction
13	Remarks	
14	Faculty Signature with Date	

Expt 7

-	**Experiment No.:**	1	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Parity Generator and Parity Checker						
2	Course Outcomes							
3	Aim	To design and verify Truth Table of 3-bit Parity Generator and 4-bit Parity Checker using basic Logic Gates with an even parity bit						
4	Material / Equipment Required	1.IC 7404, IC7432, IC7408 2. Patch chords 3.Power chords 4.Trainer Kit						
5	Theory, Formula, Principle, Concept	Theory :Parity Generator and Checker A parity generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called parity checker. The sum of the data bits and parity bits can be even or odd . In even parity, the added parity bit will make the total number of 1s an even amount whereas in odd parity the added parity bit will make the total number of 1s odd amount. In even parity bit scheme, the parity bit is '0' if there are even number of 1s in the data stream and the parity bit is '1' if there are odd number of 1s in the data stream. In odd parity bit scheme, the parity bit is '1' if there are even number of 1s in the data stream and the parity bit is '0' if there are odd number of 1s in the data stream. Let us discuss both even and odd parity generators. 3 bit Parity Generator Let us assume that a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuits and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P. The figure below shows the truth table of even parity generator in which 1 is placed as parity bit in order to make all 1s as even when the number of 1s in the truth table is odd.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe outputs						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	Parity Generator 				Parity Checker 		
	Observation Table, Look-up Table, Output	Parity Generator				Parity Checker		

		<table><tr><th colspan="3">3-bit message</th><th>Even parity bit generator (P)</th></tr><tr><th>A</th><th>B</th><th>C</th><th>Y</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td></tr></table> <table><tr><th colspan="4">4-bit received message</th><th rowspan="2">Parity error check C_p</th></tr><tr><th>A</th><th>B</th><th>C</th><th>P</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>
	Sample Calculations	
10	Graphs, Outputs	Respective Truth tables are verified
11	Results & Analysis	
12	Application Areas	Parity generators and checkers are used in error detection and correction techniques in networking systems
13	Remarks	
14	Faculty Signature with Date	

Expt 8

-	**Experiment No.:**	8a	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Master Slave Flip Flop						
2	Course Outcomes	Realize boolean expressions using multiplexer IC						
3	Aim	Realize a J-K Master / Slave Flip-Flop using NAND gates and verify its truth table.						
4	Material / Equipment Required	1. IC 74LS10 2. IC 74LS00 3. Patch chords 4. Power chords 5. Trainer Kit						
5	Theory, Formula, Principle, Concept	The control inputs to a clocked flip flop will be making a transition at approximately the same times as triggering edge of the clock input occurs. This can lead to unpredictable triggering. A JK master flip flop is positive edge triggered, where as slave is negative edge triggered. Therefore master first responds to J and K inputs and then slave. If J=0 and K=1, master resets on arrival of positive clock edge. High output of the master drives the K input of the slave. For the trailing edge of the clock pulse the slave is forced to reset. If both the inputs are high, it changes the state or toggles on the arrival of the positive clock edge and the slave toggles on the negative clock edge. The slave does exactly what the master does.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1.Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe output						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
	Observation Table, Look-up Table, Output	Function Table :						

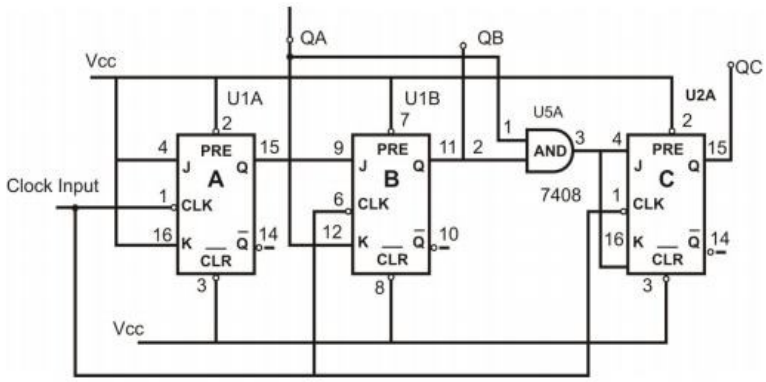
Clock	J	K	Q	Q`	Comment
Π	0	0	Q_0	Q_0`	No Change
Π	0	1	0	1	Reset
Π	1	0	1	0	Set
Π	1	1	Q_0	Q_0	Toggle

	Sample Calculations	
10	Graphs, Outputs	Respective Truth tables are verified
11	Results & Analysis	
12	Application Areas	Flip flops are used in memory devices
13	Remarks	
14	Faculty Signature with Date	

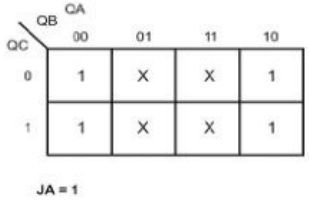
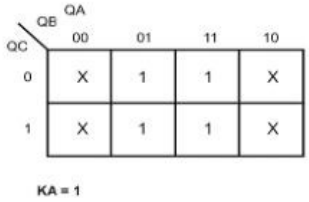
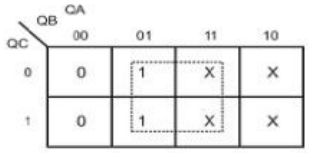
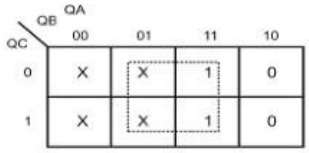
Expt 8

-	**Experiment No.:**	8b	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	D Flip-Flop with positive-edge triggering.						
2	Course Outcomes	Design and develop the Verilog / VHDL code for D Flip-Flop with positive-edge triggering. Simulate and verify its working.						
3	Aim	D Flip-Flop with positive-edge triggering..						
4	Material / Equipment Required	1. Desininging software tool						
5	Theory, Formula, Principle, Concept	It also has two outputs, with one being logically inverse of other. The data input is either logic 0 or 1, meaning low or high voltage. The clock input helps in synchronizing the circuit to an external signal. The set input and reset input are mostly held low. A D-type flip-flop can have two possible values. When input D = 0, the flip-flop undergoes a reset, which means the output would be set to 0. When input D = 1, the flip-flop does a set, which makes the output 1						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Create a new project 2. Create a new worksheet 3. Create a new blank page 4. Enter the user name and input output variable details 5. Create a new VHDL source Type the code as given						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
	Observation Table, Look-up Table, Output							
	Sample Calculations							
10	Graphs, Outputs	Respective Truth tables are verified						
11	Results & Analysis							
12	Application Areas	Flip flops are used in memory devices						
13	Remarks							
14	Faculty Signature with Date							

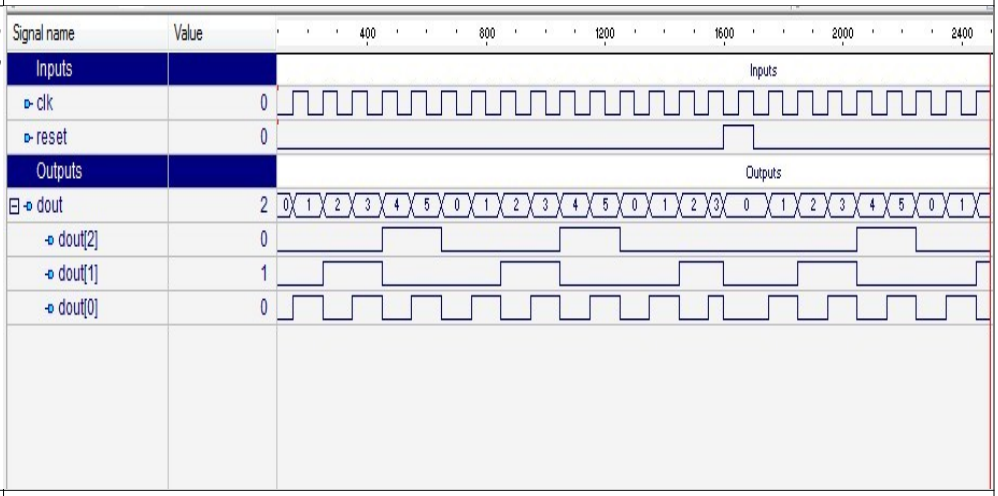
Expt 9

-	**Experiment No.:**	9a	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Synchronous counter						
2	Course Outcomes	Design and analyze synchronous counter and asynchronous counters using combination of flip flops						
3	Aim	Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop ICs and demonstrate its working						
4	Material / Equipment Required	1. IC 74LS76 2. IC 74LS08 3. Patch chords 4. Power chords 5. Trainer Kit						
5	Theory, Formula, Principle, Concept	The ripple counter requires a finite amount of time for each flip flop to change state. This problem can be solved by using a synchronous parallel counter where every flip flop is triggered in synchronism with the clock and all the output which are scheduled to change do so simultaneously. The counter progresses counting upwards in a natural binary sequence from count 000 to count 100 advancing count with every negative clock transition and get back to 000 after this cycle.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe output						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	**Circuit diagram of Mod – 8 counter:**  						
	Observation Table, Look-up Table, Output	**DESIGN FOR MOD 8 UP COUNTER:**						

Present State			Next state			Flip flop inputs					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	K_C	J_C	K_B	J_B	K_A	J_A
0	0	0	0	0	1	X	0	X	0	X	1
0	0	1	0	1	0	X	0	X	1	1	X
0	1	0	0	1	1	X	0	0	X	X	1
0	1	1	1	0	0	X	1	1	X	1	X
1	0	0	1	0	1	0	X	X	0	X	1
1	0	1	1	1	0	0	X	X	1	1	X
1	1	0	1	1	1	0	X	0	X	X	1
1	1	1	0	0	0	1	X	1	X	1	X

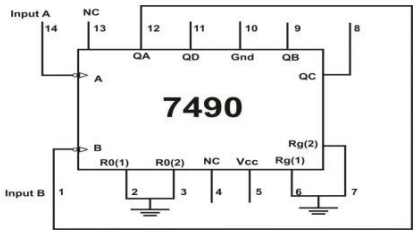
9	Sample Calculations	**Design:** **JA**  QB QA / QC 00 01 11 10 0: 1 X X 1 1: 1 X X 1 **JA = 1** **KA**  QB QA / QC 00 01 11 10 0: X 1 1 X 1: X 1 1 X **KA = 1** **JB**  QB QA / QC 00 01 11 10 0: 0 1 X X 1: 0 1 X X **JB = QA** **KB**  QB QA / QC 00 01 11 10 0: X X 1 0 1: X X 1 0 **KB = QA**
10	Graphs, Outputs	Respective Truth tables are verified
11	Results & Analysis	
12	Application Areas	Counters are used in digital clock
13	Remarks	
14	Faculty Signature with Date	

Expt 9

-	**Experiment No.:**	9b	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	mod-8 up counter						
2	Course Outcomes	Design and develop the Verilog / VHDL code for mod-8 up counter. Simulate and verify its working						
3	Aim	VHDL code for mod-8 up counter						
4	Material / Equipment Required	1. Designing software tool						
5	Theory, Formula, Principle, Concept	Then counters are sequential logic devices that follow a predetermined sequence of counting states which are triggered by an external clock (CLK) signal. The number of states or counting sequences through which a particular counter advances before returning once again back to its original first state is called the **modulus** (MOD). In other words, the modulus (or just modulo) is the number of states the counter counts and is the dividing number of the counter.						
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1. Create a new project 2. Create a new worksheet 3. Create a new blank page 4. Enter the user name and input output variable details 5. Create a new VHDL source Type the code as given						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
	Observation Table, Look-up Table, Output							
9	Sample Calculations							
10	Graphs, Outputs	Respective Truth tables are verified						
11	Results & Analysis							
12	Application Areas	Counters are used in digital clock						
13	Remarks							
14	Faculty Signature with Date							

Expt 10

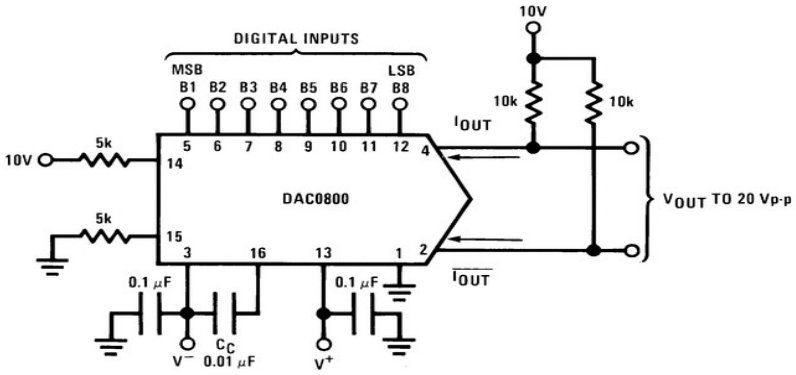
-	**Experiment No.:**	10	**Marks**		**Date Planned**		**Date Conducted**	

1	Title	Asynchronous counter
2	Course Outcomes	Design and analyze synchronous counter and asynchronous counters using combination of flip flops
3	Aim	Design and implement an asynchronous counter using decade counter IC to count up from 0 to n(n<=9) and demonstrate on 7-segment display (using IC-7447).
4	Material / Equipment Required	1.IC7490, IC7443 2. Patch chords 3.Power chords 4.Trainer Kit
5	Theory, Formula, Principle, Concept	Asynchronous counter is a counter in which the clock signal is connected to the clock input of only first stage flip flop. The clock input of the second stage flip flop is triggered by the output of the first stage flip flop and so on. This introduces an inherent propagation delay time through a flip flop. A transition of input clock pulse and a transition of the output of a flip flop can never occur exactly at the same time. Therefore, the two flip flops are never simultaneously triggered, which results in asynchronous counter operation.
6	Procedure, Program, Activity, Algorithm, Pseudo Code	1Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe output
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph	
8	Observation Table, Look-up Table, Output	

Clock	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0

		7	1	0	0	0
		8	1	0	0	1
9	Sample Calculations					
10	Graphs, Outputs	Respective Truth tables are verified				
11	Results & Analysis					
12	Application Areas	Counters are used in digital clock				
13	Remarks					
14	Faculty Signature with Date					

Expt 11

-	**Experiment No.:**	10	**Marks**		**Date Planned**		**Date Conducted**	
1	Title	Digital to analog converter						
2	Course Outcomes	Generate ramp waveform by DAC using counter IC						
3	Aim	Generate a Ramp output waveform using DAC0800 (Inputs are given to DAC through IC74393 dual 4-bit binary counter).						
4	Material / Equipment Required	DAC0800, IC74393, Trainer Kit, Patch chords , CRO						
5	Theory, Formula, Principle, Concept							
6	Procedure, Program, Activity, Algorithm, Pseudo Code	.Verify all components and patch chords whether they are in good condition or not. 2. Make connections as shown in the circuit diagram. 3. Give supply to the trainer kit. 4. Provide input data to the circuit via switches. 5. Verify truth table sequence and observe outpu						
7	Block, Circuit, Model Diagram, Reaction Equation, Expected Graph							
8	Observation Table, Look-up Table, Output							
9	Sample Calculations							
10	Graphs, Outputs							
11	Results & Analysis							
12	Application Areas	DAC are used in data transmission						
13	Remarks							
14	Faculty Signature with Date							